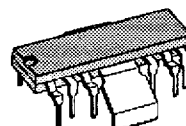


TV VERTICAL DEFLECTION

- SYNCHRONIZATION CIRCUIT
- OSCILLATOR AND RAMP GENERATOR
- HIGH POWER GAIN AMPLIFIER
- FLYBACK GENERATOR
- VOLTAGE REGULATOR



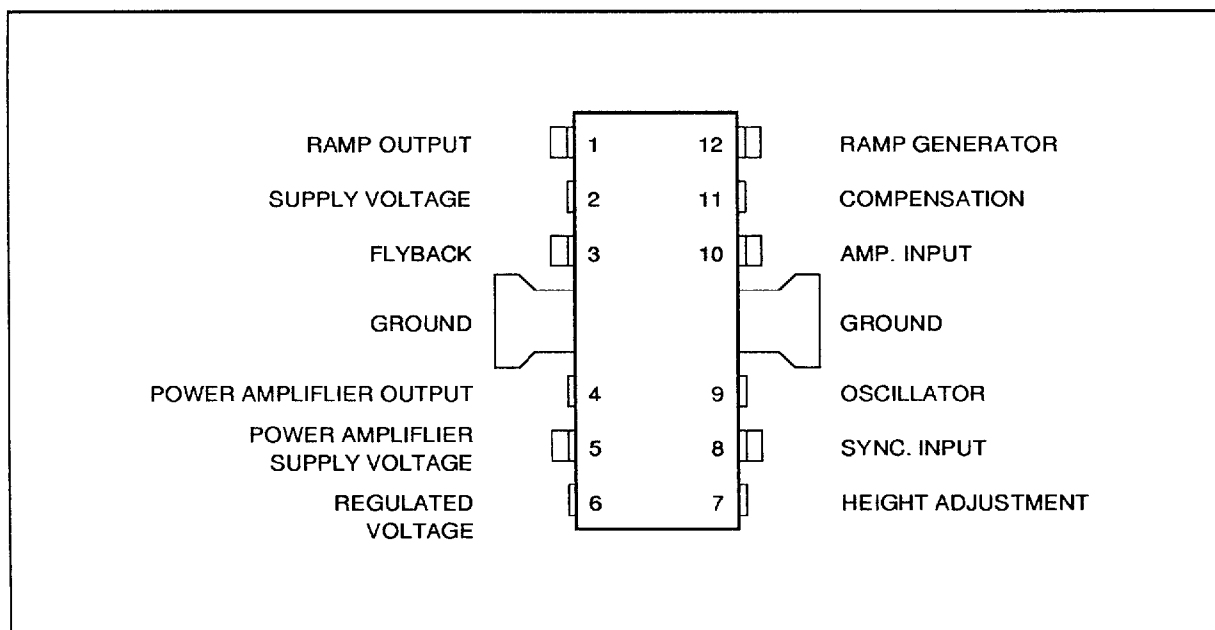
FINDIP
(Plastic Package)

ORDER CODE : TDA1170S

DESCRIPTION

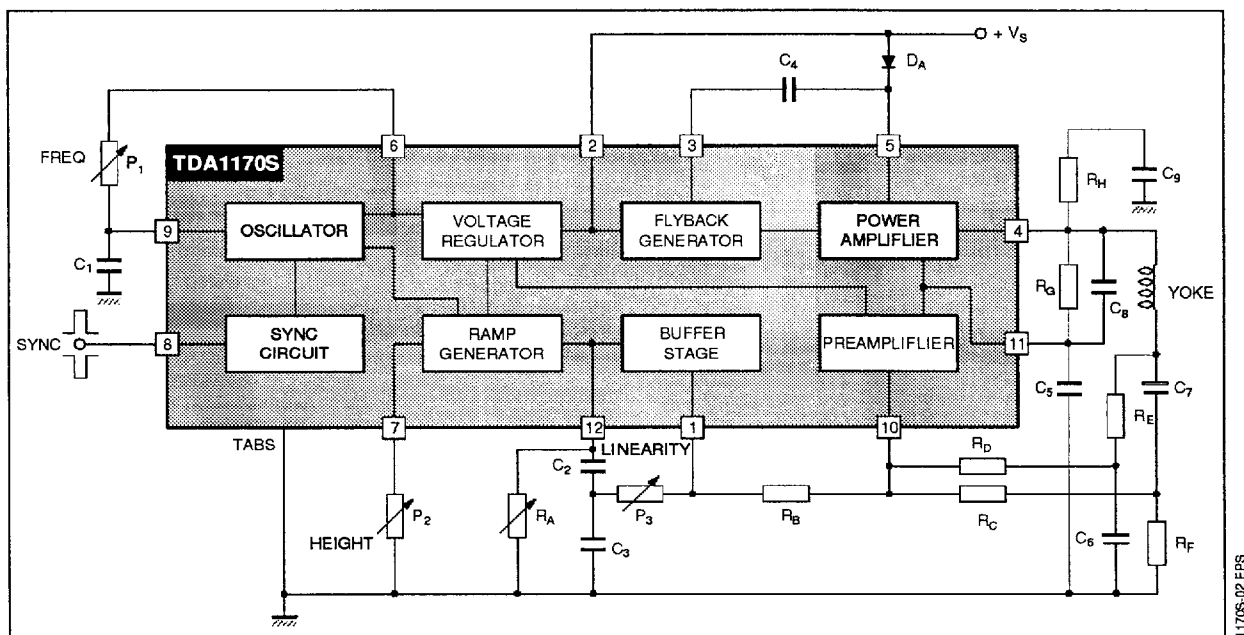
The TDA1170S is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers.

PIN CONNECTIONS

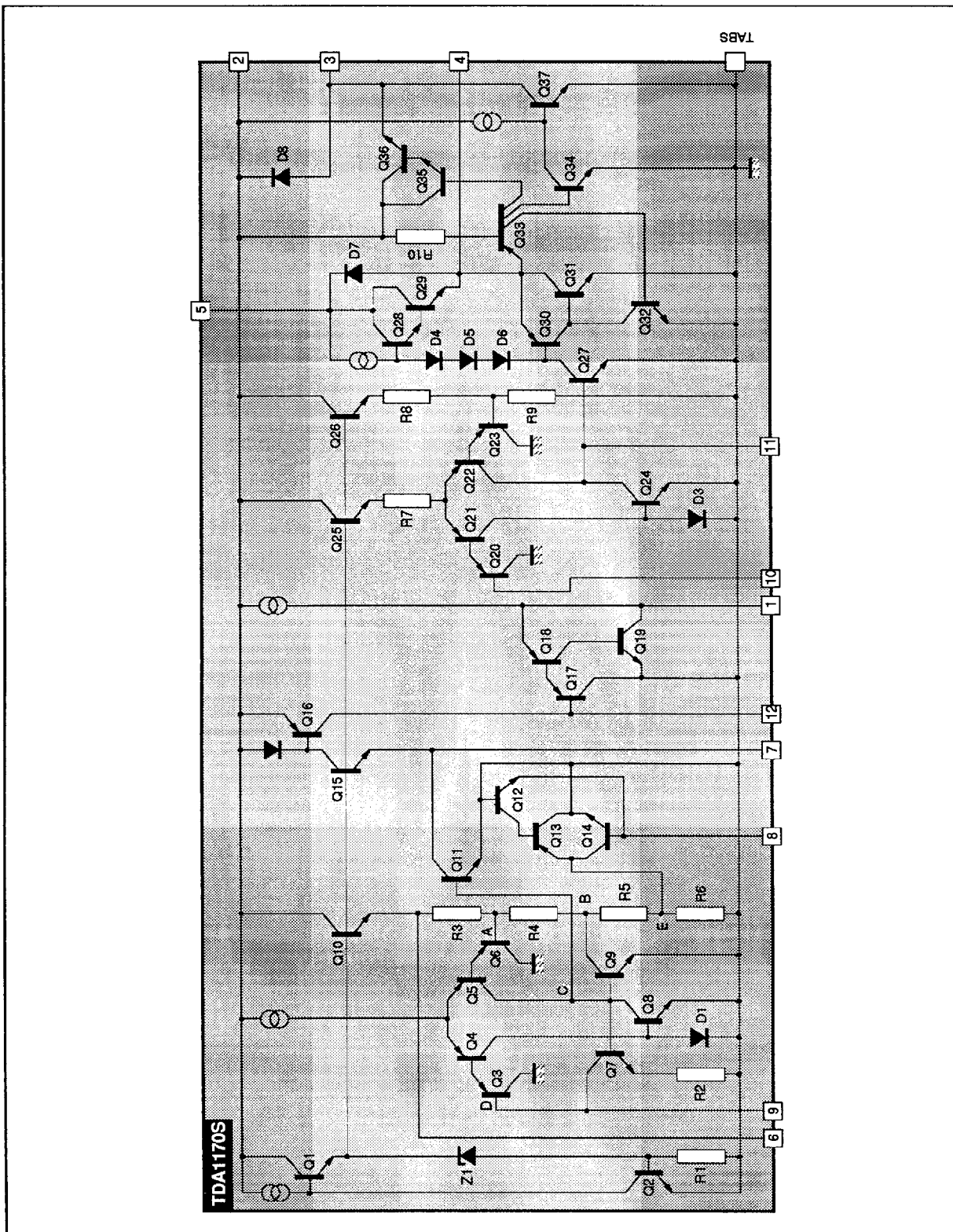


1170S-01 EPS

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



1170S-08 ERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_4, V_5	Flyback Peak Voltage	60	V
V_{10}	Power Amplifier Input Voltage	+ 10 - 0.5	V V
I_o	Output Peak Current (non repetitive) at $t = 2\text{msec}$	2	A
I_o	Output Peak Current at $f = 50\text{Hz}$ $t \leq 10\mu\text{sec}$	2.5	A
I_o	Output Peak Current at $f = 50\text{Hz}$ $t > 10\mu\text{sec}$	1.5	A
I_3	Pin 3 DC Current at $V_4/2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for $f = 50\text{Hz}$, $t_{fly} \leq 1.5\text{msec}$	1.8	A
I_8	Pin 8 Current	± 20	mA
P_{tot}	Power Dissipation : at $T_{tab} = 90^\circ\text{C}$ at $T_{amb} = 80^\circ\text{C}$	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature	- 40, + 150	$^\circ\text{C}$

1170S-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-tab}$	Thermal Resistance Junction-tab Max	12	$^\circ\text{C/W}$
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient Max	70	$^\circ\text{C/W}$

1170S-02.TBL

(*) Obtained with tabs soldered to printed circuit with minimized copper area.

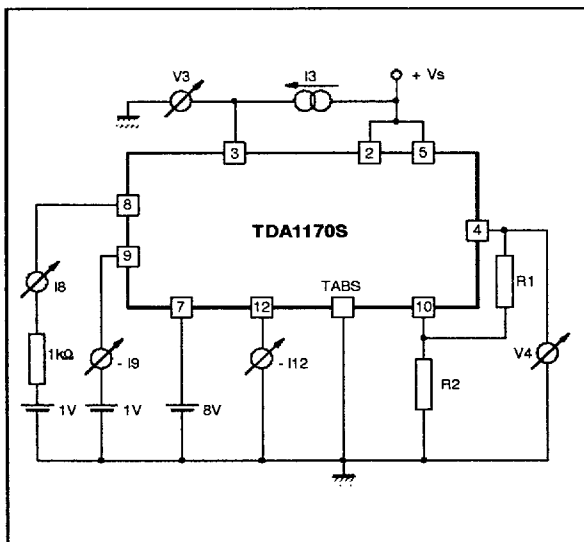
ELECTRICAL CHARACTERISTICS

(refer to the test circuits, $V_S = 35\text{V}$, $T_{amb} = 25^\circ\text{C}$, unless otherwise specified)

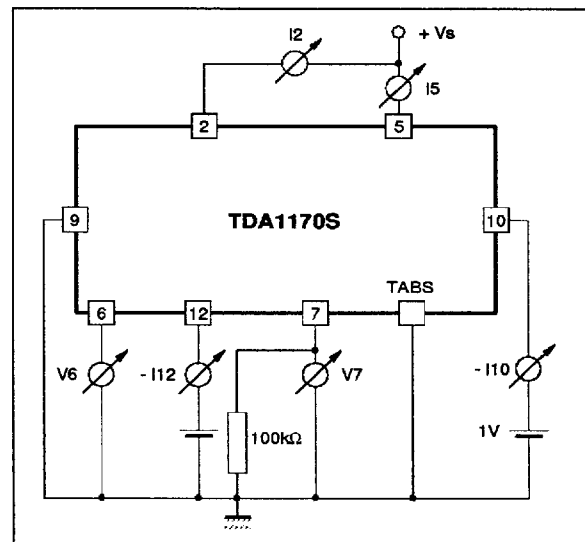
DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	15	mA	1b
$-I_9$	Oscillator Bias Current	$V_9 = 1\text{V}$		0.1	1	μA	1a
$-I_{10}$	Amplifier Input Bias Current	$V_{10} = 1\text{V}$		0.1	1	μA	1b
$-I_{12}$	Ramp Generator Bias Current	$V_{12} = 0$		0.02	0.3	μA	1a
$-I_{12}$	Ramp Generator Current	$I_7 = 20\mu\text{A}$, $V_{12} = 0$	19	20	24	μA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	$\Delta V_{12} = 0$ to 12V , $I_7 = 20\mu\text{A}$		0.2	1	%	1b
V_S	Supply Voltage Range		10		35	V	-
V_1	Pin 1 Saturation Voltage to Ground	$I_1 = 1\text{mA}$		1	1.4	V	-
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 10\text{mA}$		1.7	2.6	V	1a
V_4	Quiescent Output Voltage	$V_S = 10\text{V}$ $R_1 = 10\text{k}\Omega$, $R_2 = 10\text{k}\Omega$	4.1	4.4	4.75	V	1a
		$V_S = 35\text{V}$ $R_1 = 30\text{k}\Omega$, $R_2 = 10\text{k}\Omega$	8.3	8.8	9.45	V	1a
V_{4L}	Output Saturation Voltage to Ground	$-I_4 = 0.1\text{A}$		0.9	1.2	V	1c
		$-I_4 = 0.8\text{A}$		1.9	2.3	V	1c
V_{4H}	Output Saturation Voltage to Supply	$I_4 = 0.1\text{A}$		1.4	2.1	V	1d
		$I_4 = 0.8\text{A}$		2.8	3.2	V	1d
V_6	Regulated Voltage at Pin 6		6.1	6.5	6.9	V	1b
V_7	Regulated Voltage at Pin 7	$I_7 = 20\mu\text{A}$	6.2	6.6	7	V	1b
$\frac{\Delta V_6}{\Delta V_S}, \frac{\Delta V_7}{\Delta V_S}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_S = 10$ to 35V		1		mV/V	1b
V_{10}	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	-
R_8	Pin 8 Input Resistance	$V_8 \leq 0.4\text{V}$	1			M Ω	1a

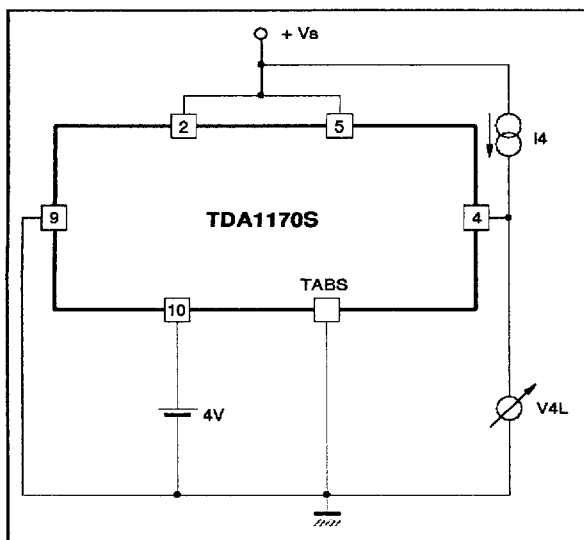
1170S-03.TBL

Figure 1 : DC Test Circuit**Figure 1a**

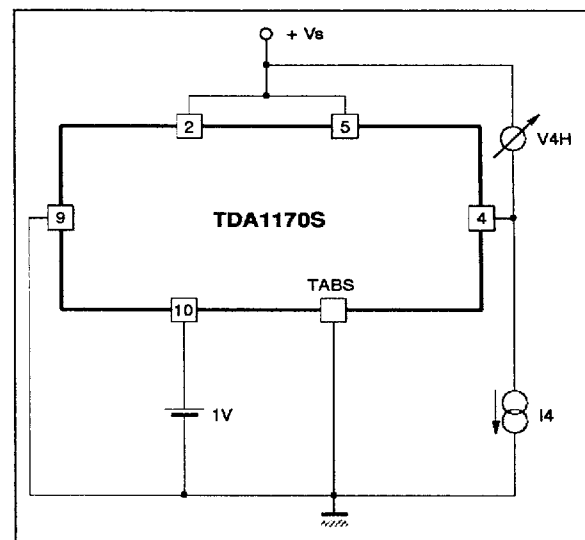
1170S-04 EPS

Figure 1b

1170S-05 EPS

Figure 1c

1170S-06 EPS

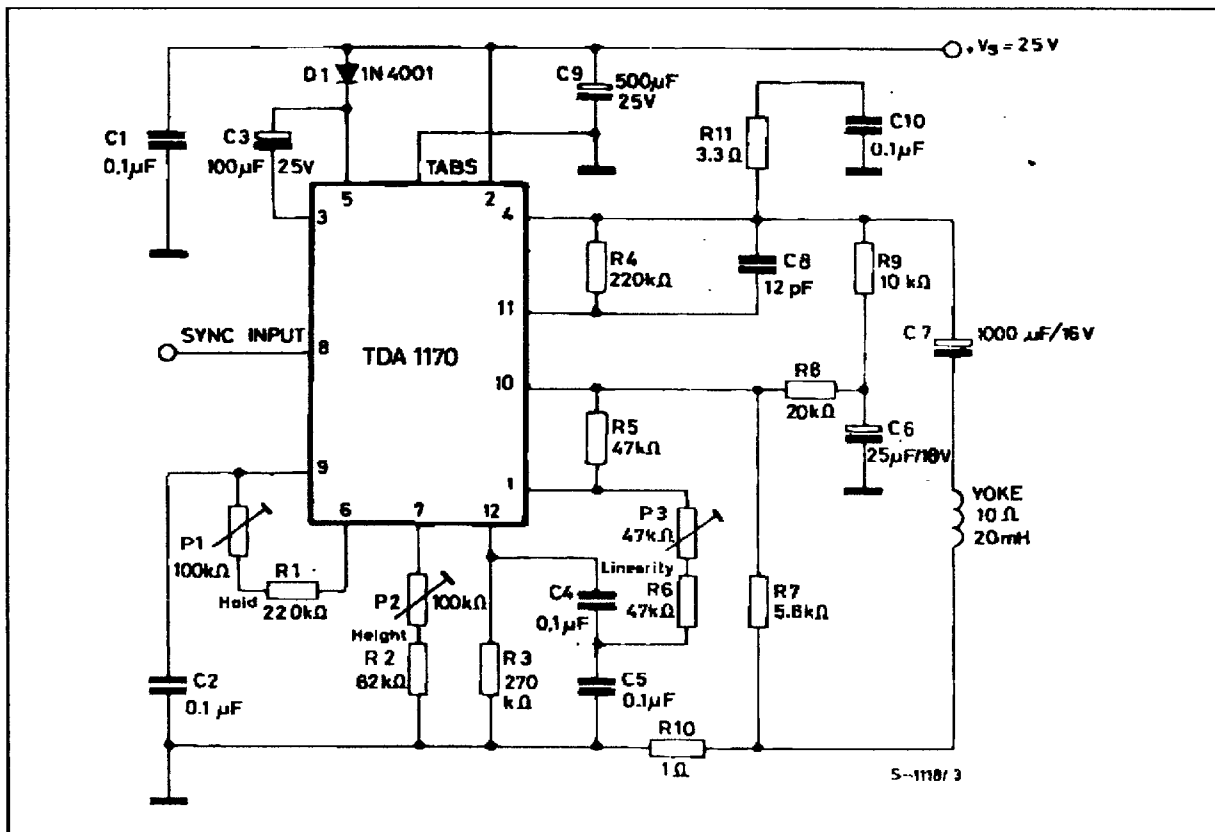
Figure 1d

1170S-07 EPS

ELECTRICAL CHARACTERISTICS(refer to the test circuit, $V_S = 25V$; $f = 50Hz$; $T_{amb} = 25^{\circ}C$, unless otherwise specified)**AC CHARACTERISTICS**

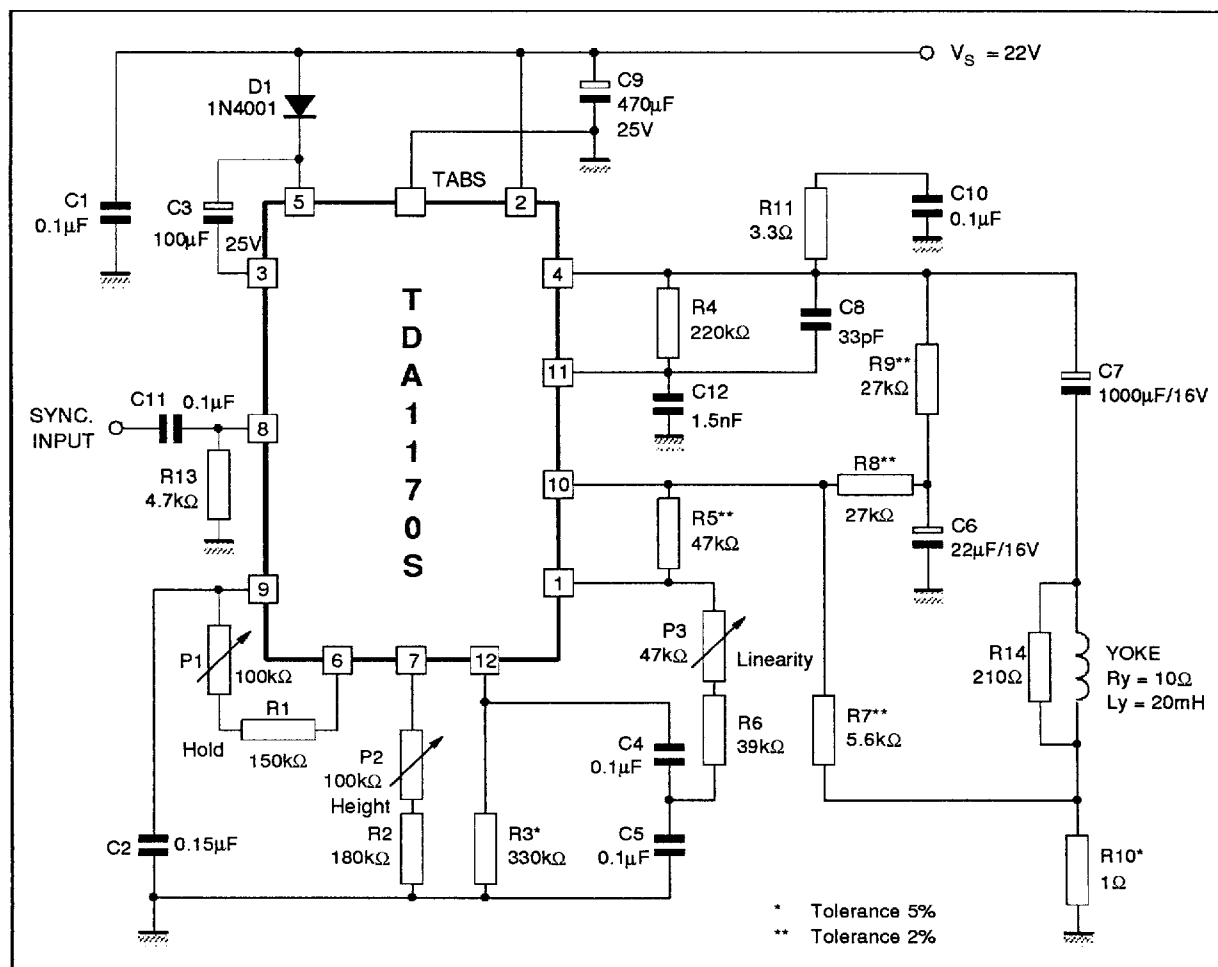
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	$I_Y = 1App$		140		mA
I_B	Sync. Input Current (positive or negative)		500			μA
V_4	Flyback Voltage	$I_Y = 1App$		51		V
V_9	Peak to Peak Oscillator Sawtooth Voltage			2.4		V
t_{fly}	Flyback Time	$I_Y = 1App$		0.7		ms
f_o	Free Running Frequency	$(P_1 + R_1) = 300k\Omega$, $C_2 = 0.1 \mu F$ $(P_1 + R_1) = 260k\Omega$, $C_2 = 0.1 \mu F$		42.2 48.5		Hz Hz
Δf	Synchronization Range	$I_B = 0.5mA$	14			Hz
$\frac{\Delta f}{\Delta V_S}$	Frequency Drift with Supply Voltage	$V_S = 10$ to $35V$		0.005		Hz/V
$\frac{\Delta f}{\Delta T_{tab}}$	Frequency Drift with Tab Temperature	$T_{tab} = 40$ to $120^{\circ}C$		0.01		Hz/ $^{\circ}C$

1170S-04.TBL

Figure 2 : AC Test Circuit

1170S-08.EPS

Figure 3 : Typical Application Circuit for Large Screen B/W TV SET ($R_Y = 10\Omega$, $L_Y = 20mH$, $I_Y = 1APP$)



TYPICAL PERFORMANCE

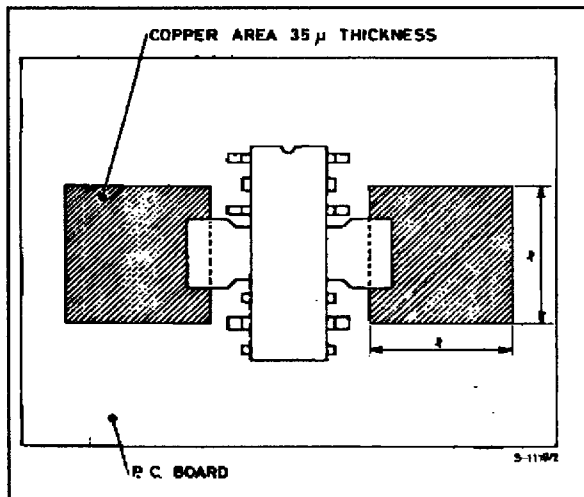
Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	22	V
I_s	Supply Current	145	mA
t_{fly}	Flyback Time	0.7	ms
P_{tot}	Power Dissipation	2.3	W
I_y	Maximum Scanning Current (peak to peak)	1.2	A

For safe working up to $T_{amb} = 60^{\circ}\text{C}$ a heatsink of $R_{th} = 14^{\circ}\text{C/W}$ is required.

MOUNTING INSTRUCTION

The junction to ambient thermal resistance of the TDA 1170S can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 4) or to an external heatsink (fig. 5).

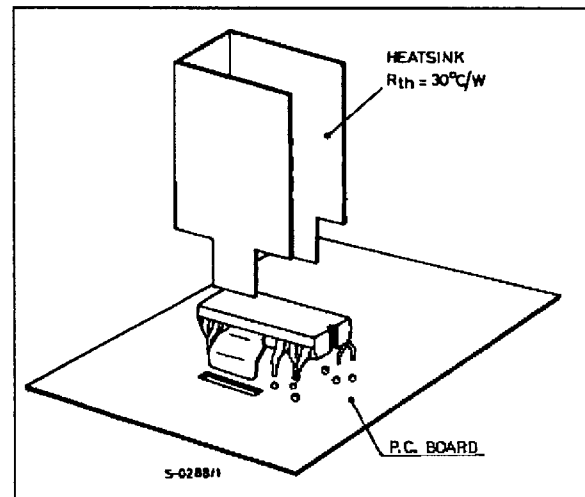
Figure 4 : Example of P.C Board Copper Area is Used as Heatsink



1170S-10.EPS

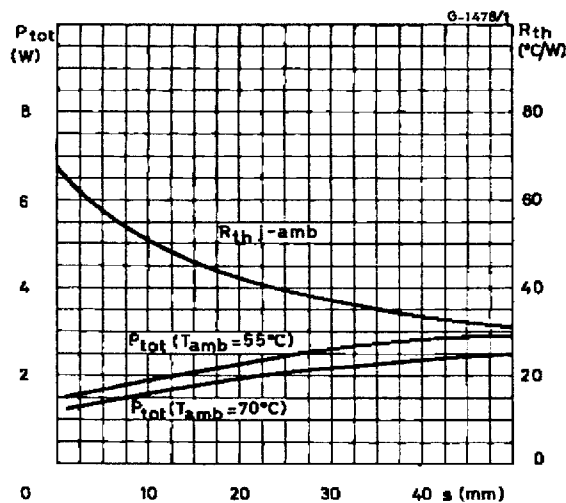
The diagram of fig. 6 shows the maximum dissippable power P_{tot} and the $R_{th j-amb}$ as a function of the side "s" of two equal square copper areas having a thickness of 35μ (1.4 mil).

Figure 5 : Example with External Heatsink



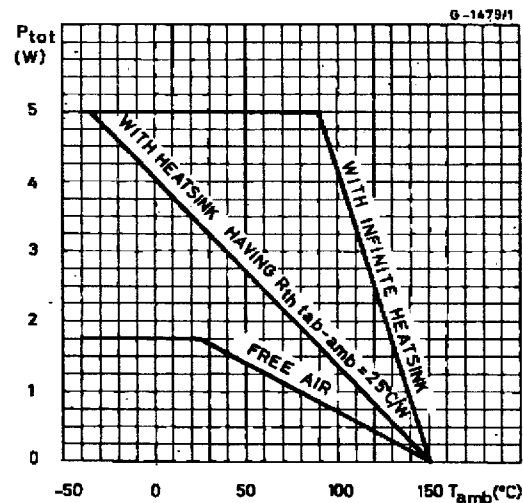
1170S-11.EPS

Figure 6 : Maximum Power Dissipation and Junction-Ambient Thermal Resistance versus "S"



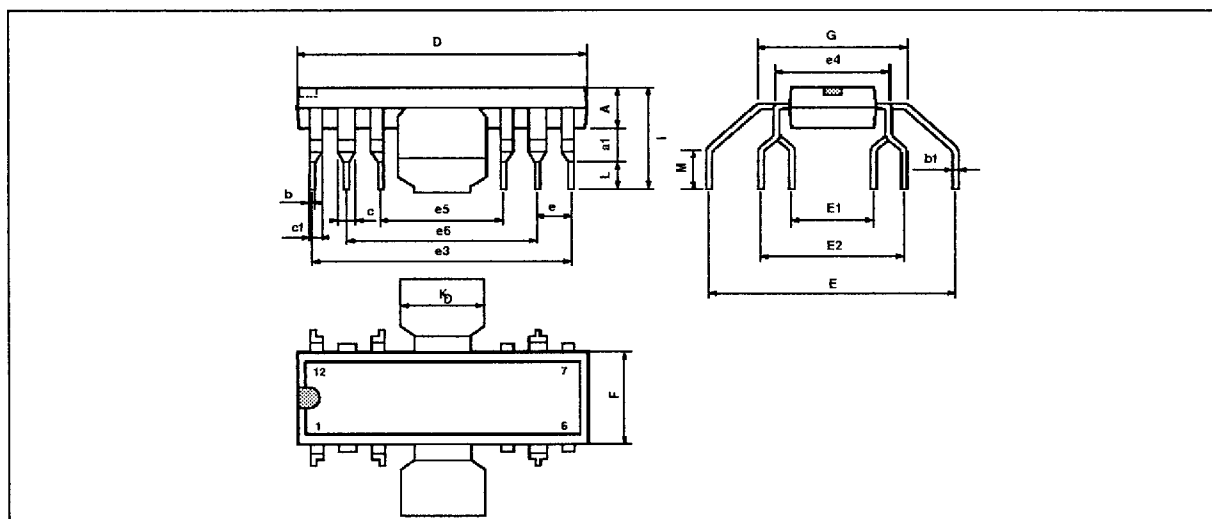
1170S-12.EPS

Figure 7 : Maximum Allowable Power Dissipation versus Ambient Temperature



1170S-13.EPS

PACKAGE MECHANICAL DATA : 12 PINS - PLASTIC FINDIP



PM-FDIP EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.8		4.05	0.150		0.159
a1	1.5		1.75	0.059		0.069
b	0.55		0.6	0.022		0.024
b1	0.3		0.35	0.012		0.014
c		1.32			0.052	
c1		0.94			0.037	
D	19.2		19.9	0.756		0.783
E	16.8	17.2	17.6	0.661	0.677	0.693
E1	4.86		5.56	0.191		0.219
E2	10.11		10.81	0.398		0.426
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	17.43	17.78	18.13	0.686	0.700	0.714
e4		7.62			0.300	
e5	7.27	7.62	7.97	0.286	0.300	0.314
e6	12.35	12.7	13.05	0.486	0.500	0.514
F	6.3		7.1	0.248		0.280
G		9.8			0.386	
I	7.8		8.6	0.307		0.339
K	6.1		6.5	0.240		0.256
L	2.5		2.9	0.098		0.114
M	2.5		3.1	0.098		

FINDIP-TBL

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