# HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage ($\varphi_1$)
- internal key pulse for phase detector ($\varphi_1$) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage ($\varphi_2$)
- larger catching range obtained by coincidence detector ($\varphi_3$; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage | $V_{1-16}$ | typ. | 12 V |
| Supply current | $I_1$ | typ. | 30 mA |
| **Input signals** | | | |
| Sync separator input voltage (peak-to-peak value) | $V_{9-16(p-p)}$ | | 3 to 4 V |
| Noise separator input voltage (peak-to-peak value) | $V_{10-16(p-p)}$ | | 3 to 4 V |
| Pulse duration switch input voltage | | | |
| at t = 7 $\mu$s (thyristor driving) | $V_{4-16}$ | | 9,4 to $V_{1-16}$ V |
| at t = 14 $\mu$s + $t_d$ (transistor driving) | $V_{4-16}$ | | 0 to 3,5 V |
| at t = 0 (input 4 open or $V_{3-16}$ = 0) | $V_{4-16}$ | | 5,4 to 6,6 V |
| **Output signals** | | | |
| Vertical sync output pulse (peak-to peak value) | $V_{8-16(p-p)}$ | typ. | 11 V |
| Burst gating output pulse (peak-to-peak value) | $V_{7-16(p-p)}$ | typ. | 11 V |
| Line drive pulse (peak-to-peak value) | $V_{3-16(p-p)}$ | typ. | 10,5 V |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

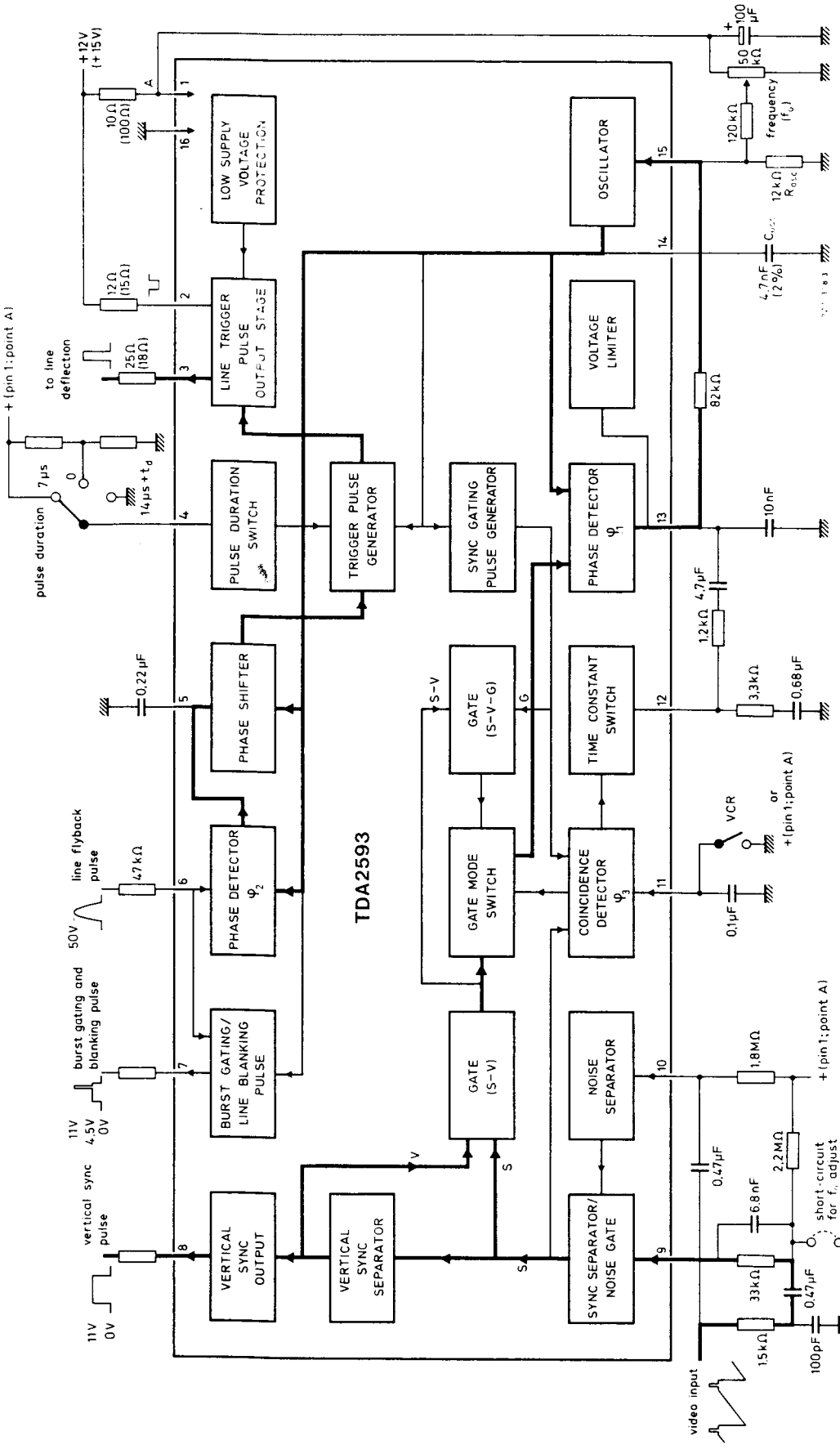


Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | | | |
| at pin 1 (voltage source) | $V_{1-16}$ | max. | 13,2 V |
| at pin 2 | $V_{2-16}$ | max. | 18 V |
| Voltages | | | |
| Pin 4 | $V_{4-16}$ | max. | 13,2 V |
| Pin 9 | $\pm V_{9-16}$ | max. | 6 V |
| Pin 10 | $\pm V_{10-16}$ | max. | 6 V |
| Pin 11 | $V_{11-16}$ | max. | 13,2 V |
| Currents | | | |
| Pins 2 and 3 (thyristor driving) (peak value) | $I_{2M}, -I_{3M}$ | max. | 650 mA |
| Pins 2 and 3 (transistor driving) (peak value) | $I_{2M}, -I_{3M}$ | max. | 400 mA |
| Pin 4 | $I_4$ | max. | 1 mA |
| Pin 6 | $\pm I_6$ | max. | 10 mA |
| Pin 7 | $-I_7$ | max. | 10 mA |
| Pin 11 | $I_{11}$ | max. | 2 mA |
| Total power dissipation | $P_{tot}$ | max. | 800 mW |
| Storage temperature | $T_{stg}$ | | −25 to + 125 °C |
| Operating ambient temperature | $T_{amb}$ | | 0 to + 70 °C |

## CHARACTERISTICS at $V_{1-16}$ = 12 V; $T_{amb}$ = 25 °C; measured in Fig. 1

### Sync separator

| | | | |
|---|---|---|---|
| Input switching voltage | $V_{9-16}$ | typ. | 0,8 V |
| Input keying current | $I_9$ | | 5 to 100 μA |
| Input leakage current at $V_{9-16}$ = −5 V | $I_9$ | < | 1 μA |
| Input switching current | $I_9$ | ⩽ | 5 μA |
| Switch off current | $I_9$ | > | 100 μA |
| | | typ. | 150 μA |
| Input signal (peak-to-peak value) | $V_{9-16(p-p)}$ | | 3 to 4 V* |

* Permissible range 1 to 7 V.

**Noise separator**

| | | | | |
|---|---|---|---|---|
| Input switching voltage | $V_{10-16}$ | typ. | 1,4 | V |
| Input keying current | $I_{10}$ | | 5 to 100 | μA |
| Input switching current | $I_{10}$ | > | 100 | μA |
| | | typ. | 150 | μA |
| Input leakage current at $V_{10-16} = -5$ V | $I_{10}$ | < | 1 | μA |
| Input signal (peak-to-peak value) | $V_{10-16(p-p)}$ | | 3 to 4 | V * |
| Permissible superimposed noise signal (peak-to-peak value) | $V_{10-16(p-p)}$ | < | 7 | V |

**Line flyback pulse**

| | | | | |
|---|---|---|---|---|
| Input current | $I_6$ | typ. | 1 | mA |
| | | | 0,02 to 2 | mA |
| Input switching voltage | $V_{6-16}$ | typ. | 1,4 | V |
| Input limiting voltage | $V_{6-16}$ | | −0,7 to + 1,4 | V |

**Switching on VCR**

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{11-16}$ | | 0 to 2,5 | V |
| | $V_{11-16}$ | | 9 to $V_{1-16}$ | V |
| Input current | $-I_{11}$ | < | 200 | μA |
| | $I_{11}$ | < | 2 | mA |

**Pulse duration switch**

For t = 7 μs (thyristor driving)

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{4-16}$ | | 9,4 to $V_{1-16}$ | V |
| Input current | $I_4$ | > | 200 | μA |

For t = 14 μs + $t_d$ (transistor driving)

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{4-16}$ | | 0 to 3,5 | V |
| Input current | $-I_4$ | > | 200 | μA |

For t = 0; $V_{3-16} = 0$ or input pin 4 open

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{4-16}$ | | 5,4 to 6,6 | V |
| Input current | $I_4$ | typ. | 0 | μA |

* Permissible range 1 to 7 V.

| | | | |
|---|---|---|---|
| **Vertical sync pulse** (positive-going) | | | |
| Output voltage (peak-to-peak value) | $V_{8\text{-}16(p\text{-}p)}$ | $>$ | 10 V |
| | | typ. | 11 V |
| Output resistance | $R_8$ | typ. | 2 kΩ |
| Delay between leading edge of input and output signal | $t_{on}$ | typ. | 15 μs |
| Delay between trailing edge of input and output signal | $t_{off}$ | typ. | $t_{on}$ μs |
| **Burst gating pulse** (positive-going) | | | |
| Output voltage (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | $>$ | 10 V |
| | | typ. | 11 V |
| Output resistance | $R_7$ | typ. | 70 Ω |
| Pulse duration; $V_{7\text{-}16}$ = 7 V | $t_p$ | typ. | 4 μs |
| | | | 3,7 to 4,3 μs |
| Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16}$ = 7 V | t | typ. | 2,65 μs |
| | | | 2,15 to 3,15 μs |
| Output trailing edge current | $I_7$ | typ. | 2 mA |
| **Line flyback-blanking pulse** (positive-going) | | | |
| Output voltage (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | | 4 to 5 V |
| Output resistance | $R_7$ | typ. | 70 Ω |
| Output trailing edge current | $I_7$ | typ. | 2 mA |
| **Line drive pulse** (positive-going) | | | |
| Output voltage (peak-to-peak value) | $V_{3\text{-}16(p\text{-}p)}$ | typ. | 10,5 V |
| Output resistance | | | |
| for leading edge of line pulse | $R_3$ | typ. | 2,5 Ω |
| for trailing edge of line pulse | $R_3$ | typ. | 20 Ω |
| Pulse duration (thyristor driving) | | | |
| $V_{4\text{-}16}$ = 9,4 to $V_{1\text{-}16}$ V | $t_p$ | typ. | 7 μs |
| | | | 5,5 to 8,5 μs |
| Pulse duration (transistor driving) | | | |
| $V_{4\text{-}16}$ = 0 to 4 V; $t_{fp}$ = 12 μs | $t_p$ | | 14 + $t_d$ μs* |
| Supply voltage for switching off the output pulse | $V_{1\text{-}16}$ | typ. | 4 V |
| **Overall phase relation** | | | |
| Phase relation between middle of sync pulse and the middle of the flyback pulse | t | typ. | 2,6 μs** |
| Tolerance of phase relation | $\lvert\Delta t\rvert$ | $<$ | 0,7 μs |

* $t_d$ = switch-off delay of line output stage.
** Line flyback pulse duration $t_{fp}$ = 12 μs.

| | | | | |
|---|---|---|---|---|
| The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control $\varphi_2$. If additional adjustment is applied it can be arranged by current supply at pin 5 such that | $\Delta I_5/\Delta t$ | typ. | 30 | $\mu A/\mu s$ |
| **Oscillator** | | | | |
| Threshold voltage low level | $V_{14\text{-}16}$ | typ. | 4,4 | V |
| Threshold voltage high level | $V_{14\text{-}16}$ | typ. | 7,6 | V |
| Discharge current | $\pm I_{14}$ | typ. | 0,47 | mA |
| Frequency; free running ($C_{osc}$ = 4,7 nF; $R_{osc}$ = 12 kΩ) | $f_o$ | typ. | 15,625 | kHz |
| Spread of frequency | $\Delta f_o/f_o$ | < | ± 5 | %* |
| Frequency control sensitivity | $\Delta f_o/\Delta I_{15}$ | typ. | 31 | Hz/μA |
| Adjustment range of network in circuit (Fig. 1) | $\Delta f_o/f_o$ | typ. | ± 10 | % |
| Influence of supply voltage on frequency | $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$ | < | ± 0,05 | %* |
| Change of frequency when $V_{1\text{-}16}$ drops to 5 V | $\Delta f_o$ | < | ± 10 | %* |
| Temperature coefficient of oscillator frequency | | < | $\pm 10^{-4}$ | Hz/K* |
| **Phase comparison $\varphi_1$** | | | | |
| Control voltage range | $V_{13\text{-}16}$ | | 3,8 to 8,2 | V |
| Control current (peak value) | $\pm I_{13M}$ | | 1,9 to 2,3 | mA |
| Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V | $I_{13}$ | < | 1 | μA |
| Output resistance | | | | |
| at $V_{13\text{-}16}$ = 4 to 8 V | $R_{13}$ | high ohmic | | ** |
| at $V_{13\text{-}16}$ < 3,8 V or > 8,2 V | $R_{13}$ | low ohmic | | ▲ |
| Control sensitivity | | typ. | 2 | kHz/μs |
| Catching and holding range (82 kΩ beteeen pins 13 and 15) | $\Delta f$ | typ. | ± 780 | Hz |
| Spread of catching and holding range | $\Delta(\Delta f)$ | typ. | ± 10 | %* |

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

| | | | | |
|---|---|---|---|---|
| **Phase comparison $\varphi_2$ and phase shifter** | | | | |
| Control voltage range | $V_{5\text{-}16}$ | | 5,4 to 7,6 | V |
| Control current (peak value) | $\pm I_{5M}$ | typ. | 1 | mA |
| Output resistance | | | | |
| at $V_{5\text{-}16}$ = 5,4 to 7,6 V | | | high ohmic * | |
| at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V | $R_5$ | typ. | 8 | kΩ |
| Input leakage current | | | | |
| $V_{5\text{-}16}$ = 5,4 to 7,6 V | $I_5$ | < | 5 | μA |
| Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{fp}$ = 12 μs) | $t_d$ | < | 15 | μs |
| Static control error | $\Delta t/\Delta t_d$ | < | 0,2 | % |
| **Coincidence detector $\varphi_3$** | | | | |
| Output voltage | $V_{11\text{-}16}$ | | 0,5 to 6 | V |
| Output current (peak value) | | | | |
| without coincidence | $I_{11M}$ | typ. | 0,1 | mA |
| with coincidence | $-I_{11M}$ | typ. | 0,5 | mA |
| **Time constant switch** | | | | |
| Output voltage | $V_{12\text{-}16}$ | typ. | 6 | V |
| Output current (limited) | $\pm I_{12}$ | < | 1 | mA |
| Output resistance | | | | |
| at $V_{11\text{-}16}$ = 2,5 to 7 V | $R_{12}$ | typ. | 0,1 | kΩ |
| at $V_{11\text{-}16} < 1{,}5$ V or $> 9$ V | $R_{12}$ | typ. | 60 | kΩ |
| **Internal gating pulse** | | | | |
| Pulse duration | $t_p$ | typ. | 7,5 | μs |

* Current source.