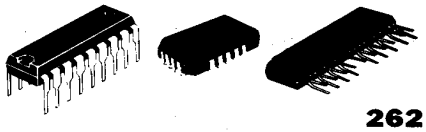


M5M4464AP, J, L-8, -10, -12, -15

262144-BIT(65536-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is family of 65536-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 18-pin package, 18-pin plastic leaded chip carrier, 20-pin zig-zag inline configuration and an increase in system densities. The M5M4464AP, J, L operates on a 5V power supply using the on-chip substrate bias generator.

FEATURES

- Performance ranges

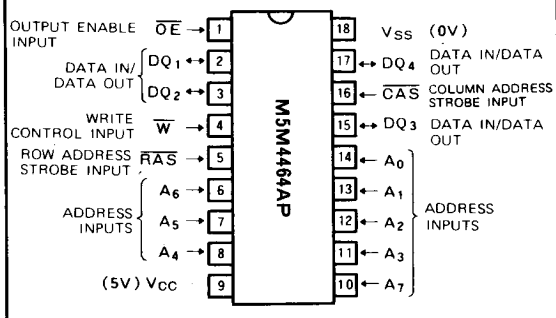
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4464A-8	80	160	300
M5M4464A-10	100	190	260
M5M4464A-12	120	220	230
M5M4464A-15	150	260	200

- 65536 x 4 Organization
- Industry standard 18-pin dual in line packages
- Single 5V±10% supply
- Low standby power dissipation . . . . . 25mW (max)
- Low operating power dissipation:
  - M5M4464AP,J,L-8 . . . . . 385mW (max)
  - M5M4464AP,J,L-10 . . . . . 360mW (max)
  - M5M4464AP,J,L-12 . . . . . 330mW (max)
  - M5M4464AP,J,L-15 . . . . . 305mW (max)
- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 256 refresh cycles/4ms
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode . . . . . 30μs max

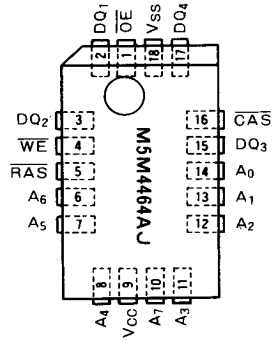
APPLICATION

Refresh memory for CRT, Micro computer memory

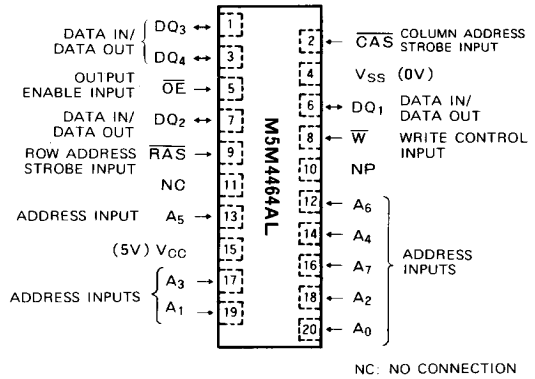
PIN CONFIGURATION (TOP VIEW)



Outline 18P4H (DIP)



Outline 18P0A (PLCC)



Outline 20P5L-A(ZIP)

MITSUBISHI ELECTRIC

FUNCTION

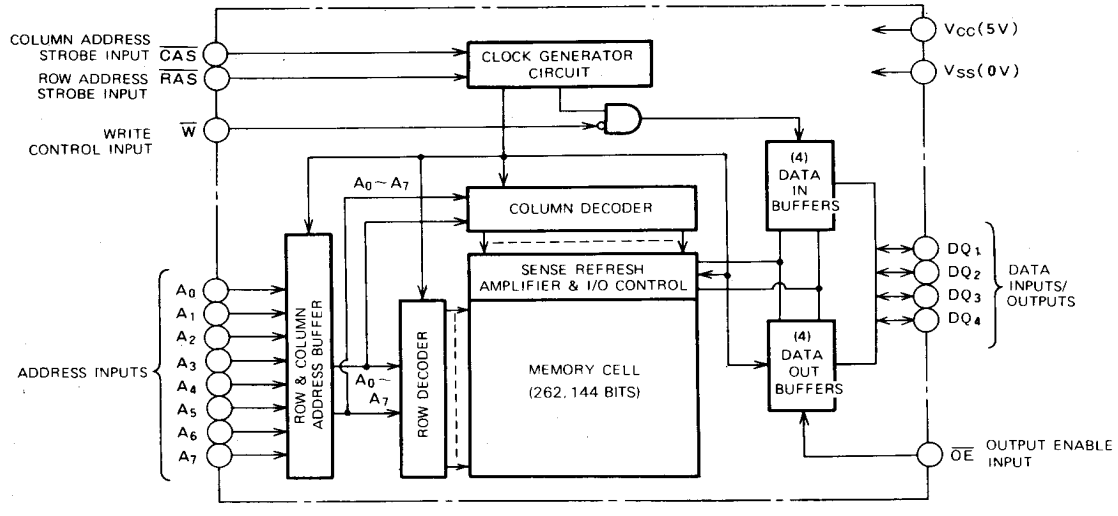
The M5M4464A provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column adress	Input DQ	Output DQ		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

BLOCK DIAGRAM



SUMMARY OF OPERATIONS

Addressing

To select one of the 262144 memory cells in the M5M4464A the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to CAS $t_{d(RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

data-in (DQ1 through DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OEHD}.

output enable ($\overline{OE}$)

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4464A must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4464A are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high

impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4464A is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4464A is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4464A as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4464A operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	parameter	Condtions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test condition	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V All other pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4464A-8	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{c(rd)}$ = $t_{c(W)}$ = min output open			70	mA
		M5M4464A-10				65	
		M5M4464A-12				60	
		M5M4464A-15				55	
$I_{CC2(AV)}$	Supply current from V_{CC}, standby		$\overline{RAS}$ = V_{IH}, output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, retreshing (Note 3)	M5M4464A-8	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} $t_{c(Prd)}$ = min output open			60	mA
		M5M4464A-10				55	
		M5M4464A-12				50	
		M5M4464A-15				45	
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5M4464A-8	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling $t_{c(Prd)}$ = min output open			55	mA
		M5M4464A-10				50	
		M5M4464A-12				45	
		M5M4464A-15				40	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4464A-8	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{c(RAS)}$ = min output open			65	mA
		M5M4464A-10				60	
		M5M4464A-12				55	
		M5M4464A-15				50	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the tastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I = V_{SS}$ f = 1MHz V_I = 25mVrms			5	pF
$C_{I(OE)}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input				10	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	Limits								Unit
				M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
				Min	Max	Min	Max	Min	Max	Min	Max	
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6, 7)	t_{CAC}		45		50		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6, 8)	t_{RAC}		80		100		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	t_{OAC}		25		25		30		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 9)	t_{OFF}	0	20	0	25	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 9)	—	0	20	0	25	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF
7: Assume that $t_{RLCL} \geqq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If t_{RLCL} is greater than t_{RLCL} max then $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 10,11)

Symbol	Parameter		Alternative Symbol	Limits								Unit
				M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
				Min	Max	Min	Max	Min	Max	Min	Max	
$t_{c(RF)}$	Refresh cycle time		t_{REF}		4		4		4		4	ms
$t_{w(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	70		80		90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	20	35	22	50	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	0		0		0		0		ns
$t_{su(RA)}$	Row address setup time before $\overline{CAS}$ low		t_{ASR}	0		0		0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	10		12		15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	15		15		20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	60		65		80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	3	50	3	50	ns

Note 10: The timing requirements are assumed t_T = 5ns.
11: V_{IH} min V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; if t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$, if t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(R)}$. t_{RLCL} min is specified as t_{RLCL} min = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is applicable for $\overline{RAS}/\overline{CAS}$ cycles.
14: t_T is measured between V_{IH} min V_{IL} max.

Read and Refresh Cycles

Symbol	Parameter		Alternative Symbol	Limit								Unit
				M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
				Min	Max	Min	Max	Min	Max	Min	Max	
$t_{c(rd)}$	Read cycle time		t_{RC}	160		190		220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	80	10000	100	10000	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	45	100000	50	100000	60	100000	75	100000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	20		22		25		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	80		100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	45		50		60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	(Note 15)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	(Note 15)	t_{RRH}	10		10		10		10		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		—	20		25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		t_{OES}	0		0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		—	45		50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	80		100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	20		25		25		30		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		—	0		0		0		0		ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

Write Cycles (Early Write and Delayed Write)

Symbol	Parameter	Alternative Symbol	Limit								Unit
			M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{c(w)}$	Write cycle time	t_{RC}	160		190		220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	80	10000	100	10000	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	40	100000	50	100000	60	100000	75	100000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	20		22		25		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	80		100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	45		50		60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		−5		−5		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	30		35		40		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	80		85		100		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	30		35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	30		35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	30		35		40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	30		35		40		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	30		35		40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	80		85		90		110		ns
t_{OEHD}	Data time, $\overline{OE}$ high to Data	—	20		25		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after Write low	—	20		25		25		30		ns

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Read-Write and Read-Modify Write Cycles

Symbol	Parameter	Alternative Symbol	Limit								Unit
			M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{C(rdW)}$	Read write/read modify write cycle time (Note 16)	t_{RWC}	220		260		295		345		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	t_{RAWS}	140	10000	170	10000	195	10000	235	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	105	100000	120	100000	135	100000	160	100000	ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	140		170		195		235		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	105		120		135		160		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	20		22		25		30		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low	t_{CWL}	30		35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low	t_{RWL}	30		35		40		45		ns
$t_{W(W)}$	Write pulse width	t_{WP}	30		35		40		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		0		ns
$t_{h(WLD)}$	Data hold time after Write low	t_{DH}	30		35		40		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	—	40		50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	80		100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	—	20		25		25		30		ns

Note 16: $t_{C(rdw)}$ is specified as $t_{C(rdw)}$ min = $t_{a(R)}$ max + t_{OEHD} min + $t_{h(WRH)}$ min + $t_{W(RH)}$ min + $4t_T$.

Page-Mode Cycle (Note 17)

Symbol	Parameter	Alternative Symbol	Limit								Unit
			M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time	t_{PC}	80		100		120		145		ns
$t_{C(PW)}$	Write cycle time	t_{PC}	80		100		120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 18)	t_{RAS}	160	30000	200	30000	240	30000	290	30000	ns
$t_{C(PrdW)}$	Read write/read modify write cycle time	—	140		170		195		230		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 19)	t_{RAS}	280	30000	340	30000	390	30000	465	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CP}	30		40		50		60		ns

Note 17: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
18: Specified for read or write cycle.
19: Specified for read-write or read-modify-write cycle.

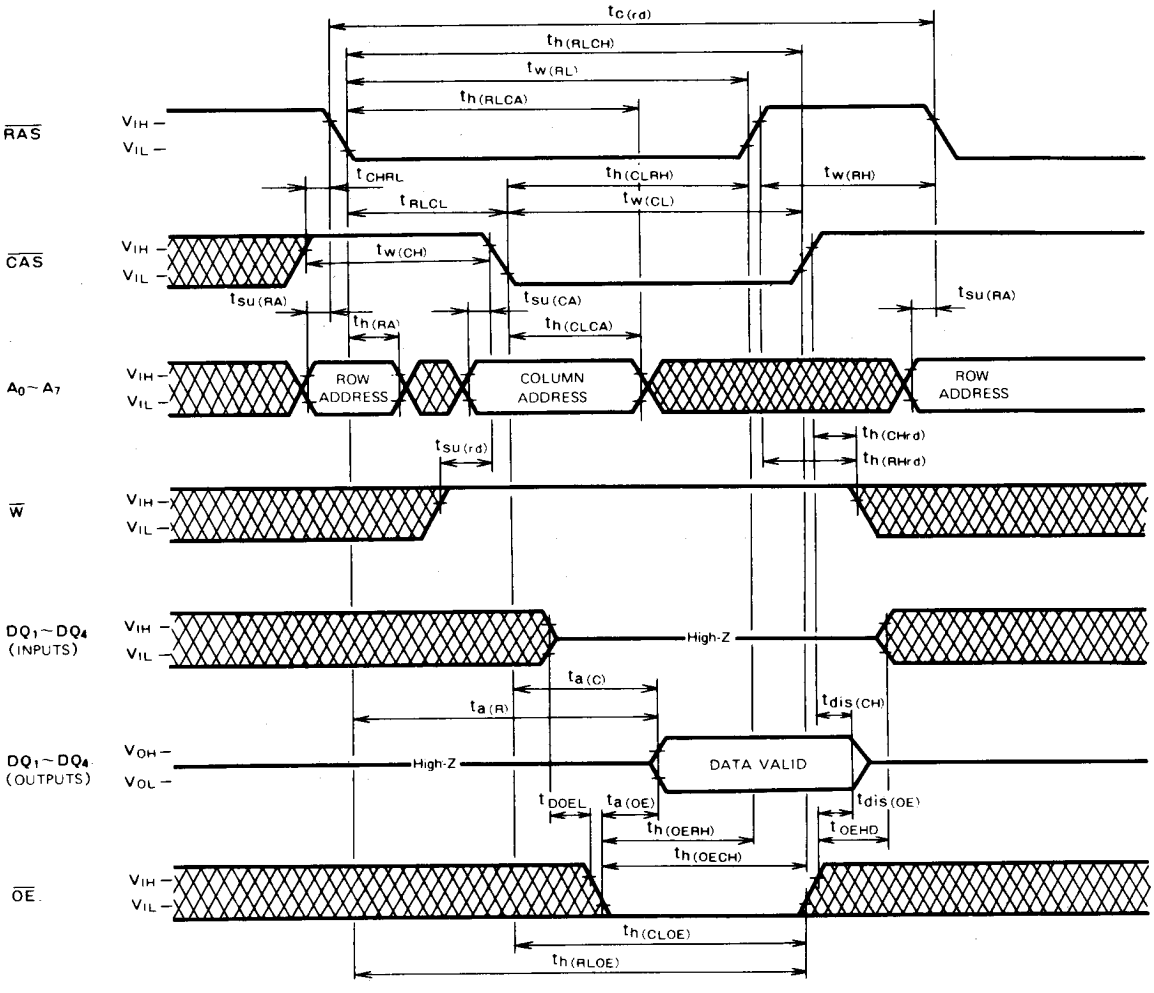
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

Symbol	Parameter	Alternative Symbol	Limit								Unit
			M5M4464A-8		M5M4464A-10		M5M4464A-12		M5M4464A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{suR(CR)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	0		0		0		0		ns
$t_{hR(RC)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	20		20		25		30		ns
$t_{dR(RC)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		0		ns

Note 20: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

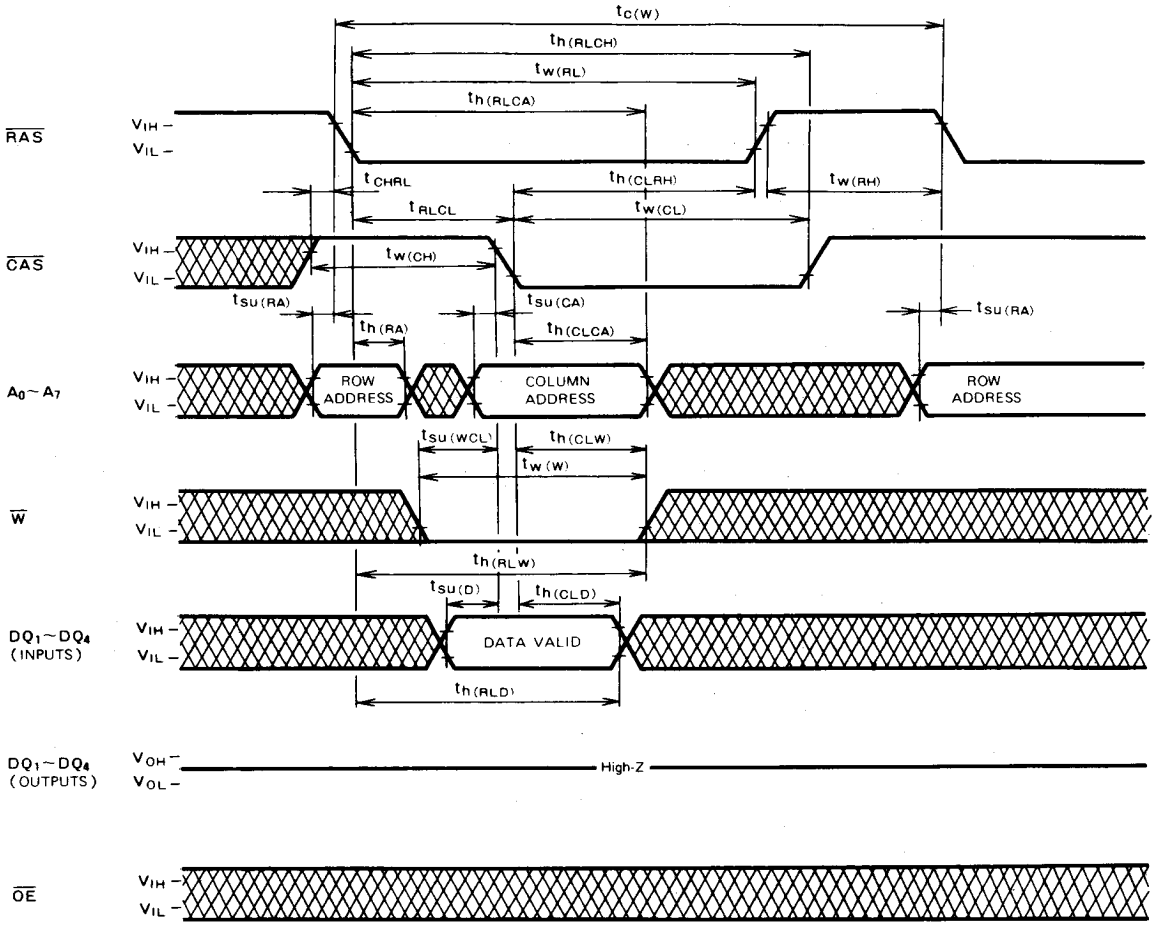
TIMING DIAGRAMS (Note 21)

Read Cycle

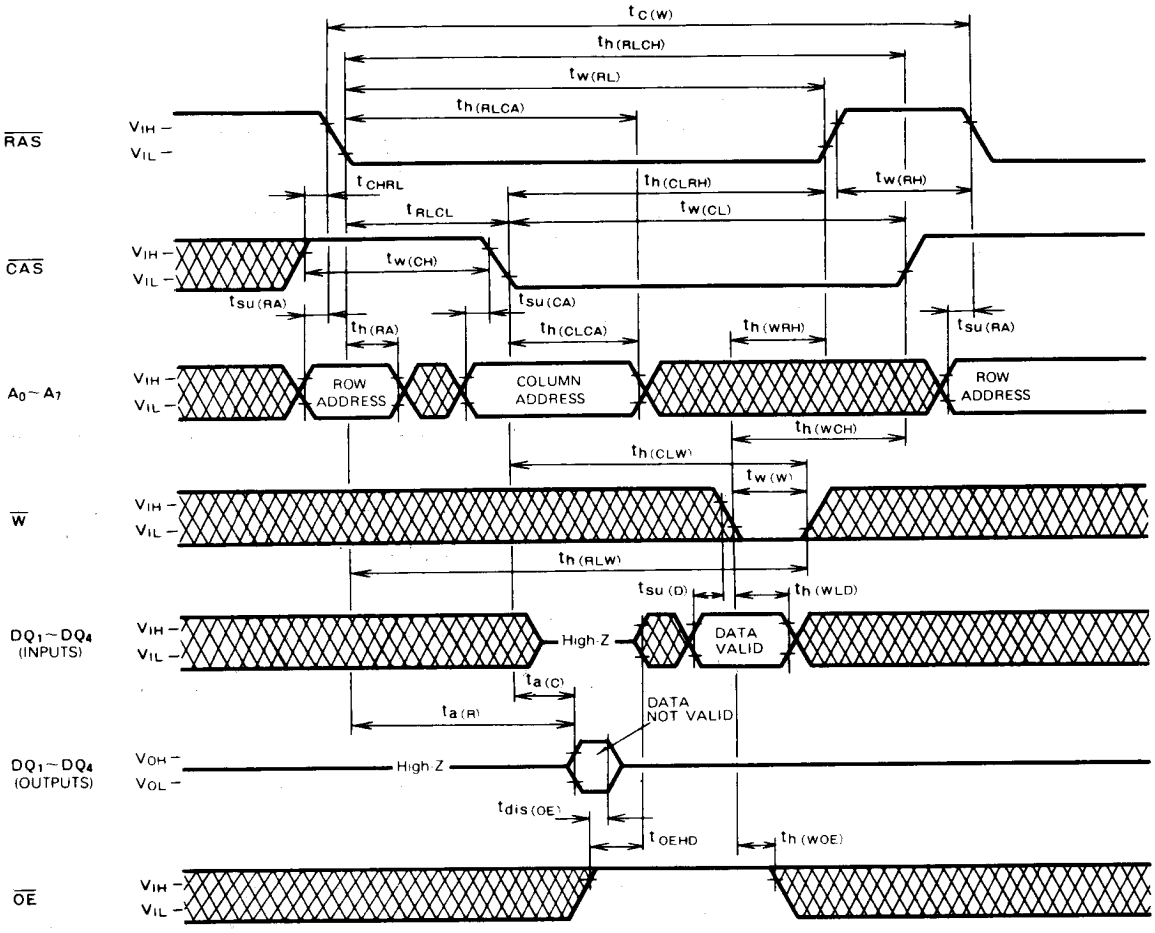


Note 21.  Indicates the don't care input.

Write Cycle (Early Write)

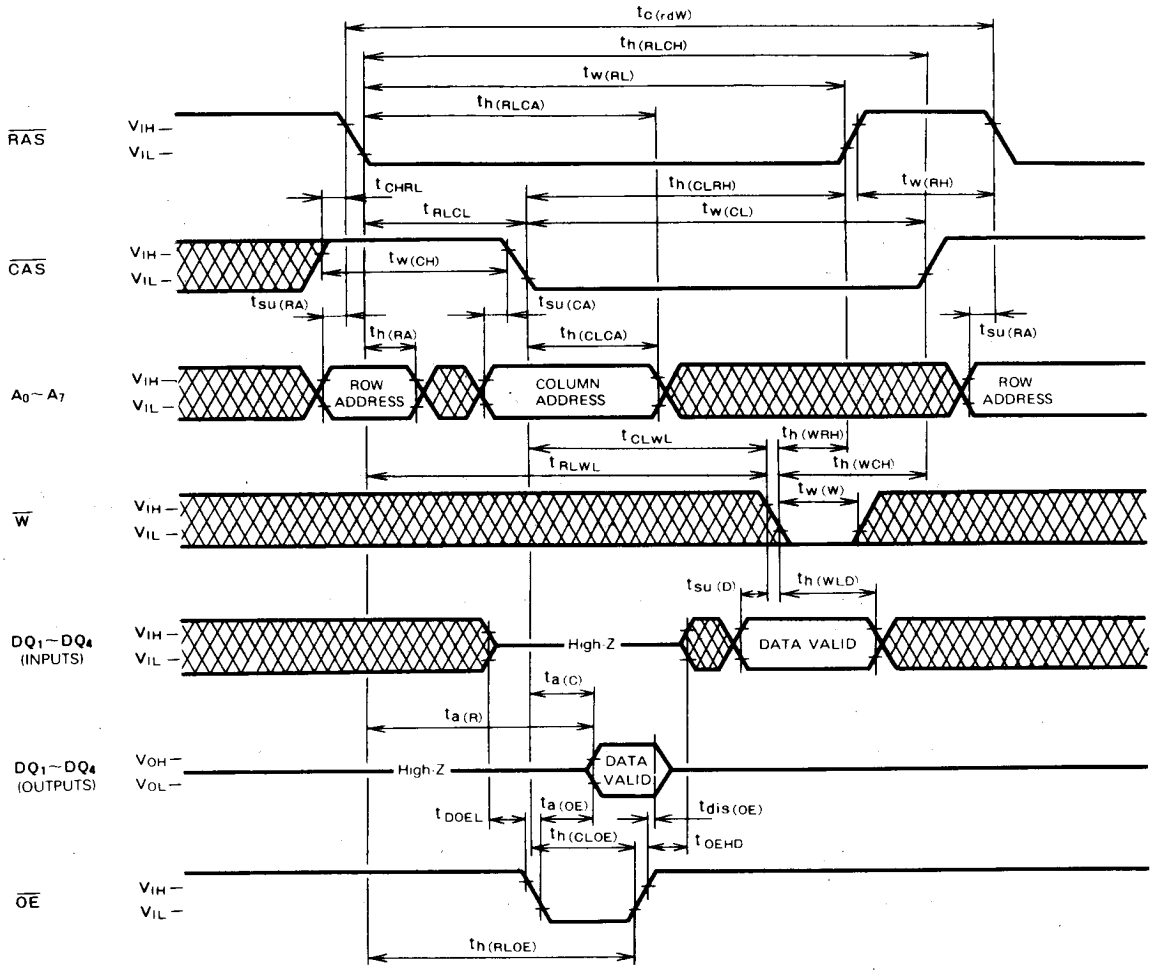


Write Cycle (Delayed Write)

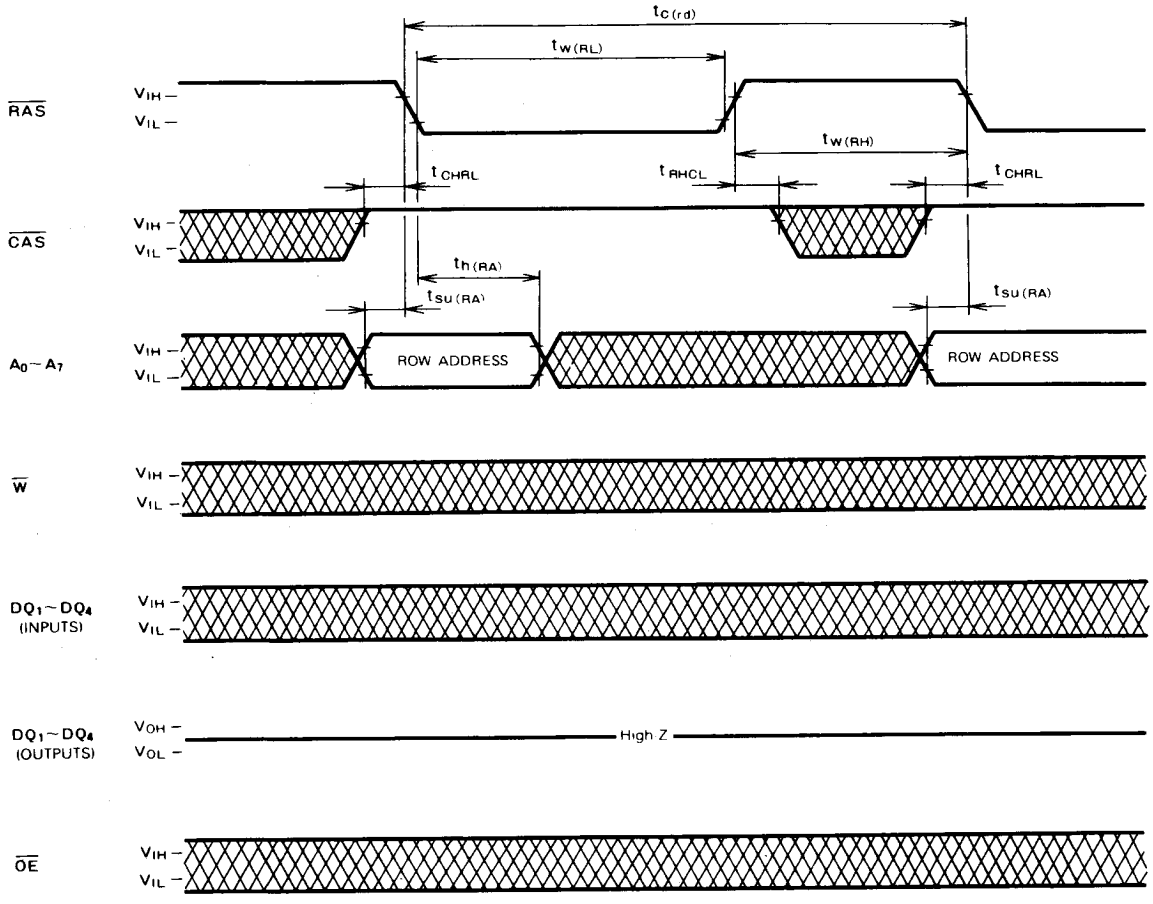


MITSUBISHI ELECTRIC

Read-Write and Read-Modify-Write Cycles

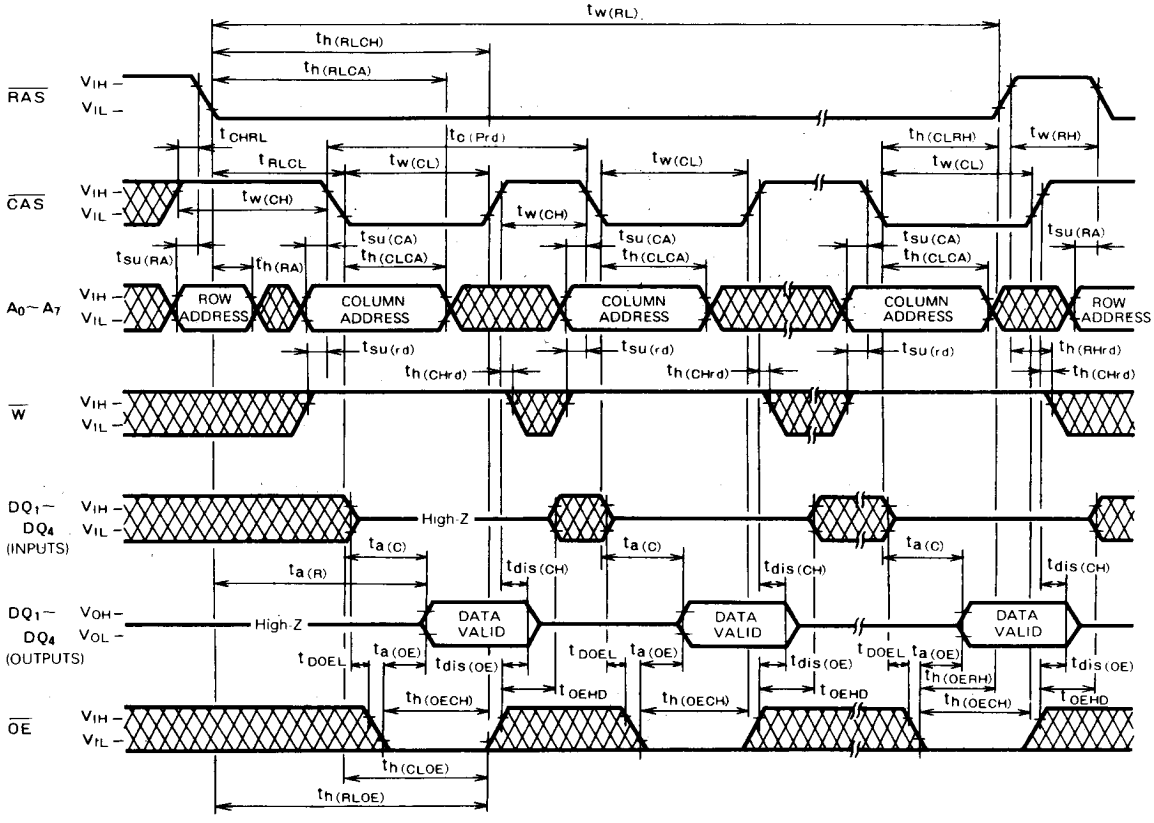


$\overline{RAS}$-Only Refresh Cycle

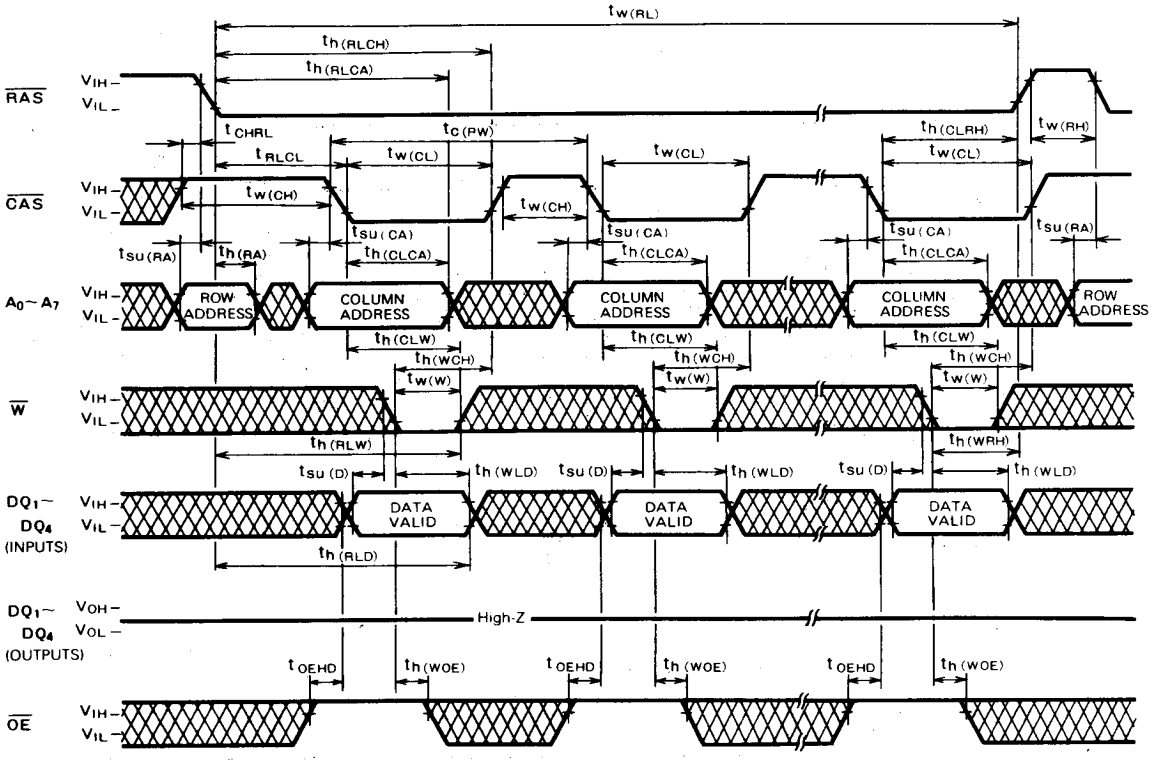


MITSUBISHI ELECTRIC

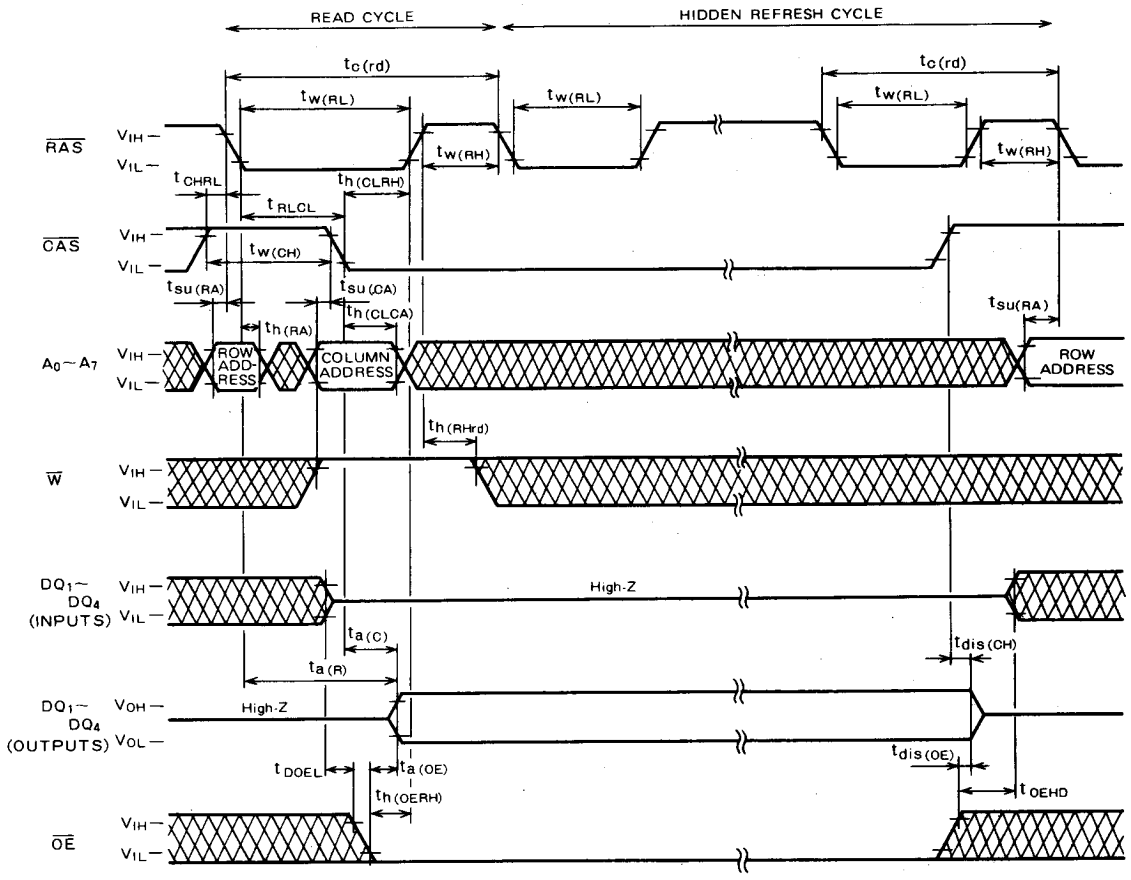
Page-Mode Read Cycle



Page-Mode Write Cycle



Hidden Refresh Cycle



CAS before RAS Refresh Cycle