

Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation Multiple Array Matrix (MAX) architecture
- 5.0-V in-system programmability (ISP) via standard Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990) available in MAX 7000S devices
- Built-in JTAG boundary-scan test (BST) circuitry in MAX® 7000S devices with 128 or more macrocells
- Complete EPLD family with logic densities ranging from 600 to 5,000 usable gates (see Table 1)
- 5-ns pin-to-pin logic delays with up to 178.6-MHz counter frequencies (including interconnect)
- PCI-compliant devices available
- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls

Table 1. MAX 7000 Device Features *Note (1)*

| Feature | EPM7032 EPM7032V EPM7032S | EPM7064 EPM7064S | EPM7096 | EPM7128E EPM7128S | EPM7160E EPM7160S | EPM7192E EPM7192S | EPM7256E EPM7256S |
|------------------------|---------------------------------|---------------------|---------|----------------------|----------------------|----------------------|----------------------|
| Usable gates | 600 | 1,250 | 1,800 | 2,500 | 3,200 | 3,750 | 5,000 |
| Macrocells | 32 | 64 | 96 | 128 | 160 | 192 | 256 |
| Logic array blocks | 2 | 4 | 6 | 8 | 10 | 12 | 16 |
| Maximum user I/O pins | 36 | 68 | 76 | 100 | 104 | 124 | 164 |
| t _{PD} (ns) | 6 (12) | 5 | 7.5 | 6 | 6 | 7.5 | 7.5 |
| t _{SU} (ns) | 5 (10) | 4 | 6 | 5 | 5 | 6 | 6 |
| t _{FSU} (ns) | 2.5 (n/a) | 2.5 | 3 | 2.5 | 2.5 | 3 | 3 |
| t _{CO1} (ns) | 4 (7) | 3.5 | 4.5 | 4 | 4 | 4.5 | 4.5 |
| f _{CNT} (MHz) | 151.5 (90.9) | 178.6 | 125 | 151.5 | 151.5 | 125 | 125 |

Note:

(1) Values in parentheses are for low-voltage EPM7032V devices.

...and More Features

- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
 - Full 3.3-V EPM7032V device
 - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
 - Pin compatible with low-voltage MAX 7000A devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
 - Six pin- or logic-driven output enable signals
 - Two global clock signals with optional inversion
 - Enhanced interconnect resources for improved routability
 - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
 - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, as well as programming hardware from third-party manufacturers

General Description

The MAX 7000 family of high-density, high-performance (PLDs) is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 178.6 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, -12P speed grades comply with the **PCI Local Bus Specification, Revision 2.1**. See [Table 2](#) for available speed grades.

Table 2. MAX 7000 Speed Grades *Note (1)*

| Device | Speed Grade | | | | | | | | | |
|----------|-------------|-------|-------|------|-------|------|-----|-------|------|-----|
| | -5 | -6 | -7 | -10P | -10 | -12P | -12 | -15 | -15T | -20 |
| EPM7032 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | |
| EPM7032V | | | | | | | ✓ | ✓ | | ✓ |
| EPM7032S | | ✓ (1) | ✓ (1) | | ✓ (1) | | | | | |
| EPM7064 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7064S | ✓ (1) | ✓ (1) | ✓ (1) | | ✓ (1) | | | | | |
| EPM7096 | | | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7128E | | | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7128S | | ✓ (1) | ✓ (1) | | ✓ (1) | | | ✓ (1) | | |
| EPM7160E | | | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7160S | | ✓ (1) | ✓ (1) | | ✓ (1) | | | ✓ (1) | | |
| EPM7192E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7192S | | | ✓ (1) | | ✓ (1) | | | ✓ (1) | | |
| EPM7256E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7256S | | | ✓ (1) | | ✓ (1) | | | ✓ (1) | | |

Note:

- (1) All information on MAX 7000S devices is preliminary. Contact Altera Customer Marketing at (408) 544-7104 for product availability.

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See [Table 3](#).

Table 3. MAX 7000 Device Features

| Feature | EPM7032 EPM7032V EPM7064 EPM7096 | All MAX 7000E Devices | All MAX 7000S Devices |
|---|---|-----------------------------|-----------------------------|
| ISP via JTAG interface | | | ✓ |
| JTAG BST circuitry | | | ✓ (1) |
| Open-drain output option | | | ✓ |
| Fast input registers | | ✓ | ✓ |
| Six global output enables | | ✓ | ✓ |
| Two global clocks | | ✓ | ✓ |
| Slew-rate control | | ✓ | ✓ |
| MultiVolt interface, Note (2) | ✓ | ✓ | ✓ |
| Programmable register | ✓ | ✓ | ✓ |
| Parallel expanders | ✓ | ✓ | ✓ |
| Shared expanders | ✓ | ✓ | ✓ |
| Power-saving mode | ✓ | ✓ | ✓ |
| Security bit | ✓ | ✓ | ✓ |
| PCI-compliant devices available | ✓ | ✓ | ✓ |

Notes:

- (1) Available in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
- (2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000 devices are an ideal alternative to gate-arrays. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 4](#).

Table 4. MAX 7000 Maximum User I/O Pins *Note (1), (2)*

| Device | 44-Pin PLCC | 44-Pin PQFP | 44-Pin TQFP | 68-Pin PLCC | 84-Pin PLCC | 100-Pin PQFP | 100-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 208-Pin RQFP |
|----------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|----------------|----------------|-----------------|-----------------|
| EPM7032 | 36 | 36 | 36 | | | | | | | | | |
| EPM7032V | 36 | | 36 | | | | | | | | | |
| EPM7032S | 36 | | 36 | | | | | | | | | |
| EPM7064 | 36 | | 36 | 52 | 68 | 68 | | | | | | |
| EPM7064S | 36 | | 36 | | 68 | | 68 | | | | | |
| EPM7096 | | | | 52 | 64 | 76 | | | | | | |
| EPM7128E | | | | | 68 | 84 | | 100 | | | | |
| EPM7128S | | | | | 68 | 84 | 84, (3) | 100 | | | | |
| EPM7160E | | | | | 64 | 84 | | 104 | | | | |
| EPM7160S | | | | | 64 | | 84, (3) | 104 | | | | |
| EPM7192E | | | | | | | | 124 | 124 | | | |
| EPM7192S | | | | | | | | 124 | | | | |
| EPM7256E | | | | | | | | 132, (3) | | 164 | | 164 |
| EPM7256S | | | | | | | | | | | 164, (3) | 164 |

Notes:

- (1) Contact Altera for up-to-date information on available device package options.
- (2) When the JTAG interface in MAX 7000S devices is used, four I/O pins become JTAG pins.
- (3) Perform a complete thermal analysis before committing a design to this device package. See the [Operating Requirements for Altera Devices Data Sheet](#) in the **1998 Data Book** for more information.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that allows schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. The MAX+PLUS II software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

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For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in the **1998 Data Book**.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7032V, EPM7064, and EPM7096 devices.

Figure 1. EPM7032, EPM7032V, EPM7064 & EPM7096 Device Block Diagram

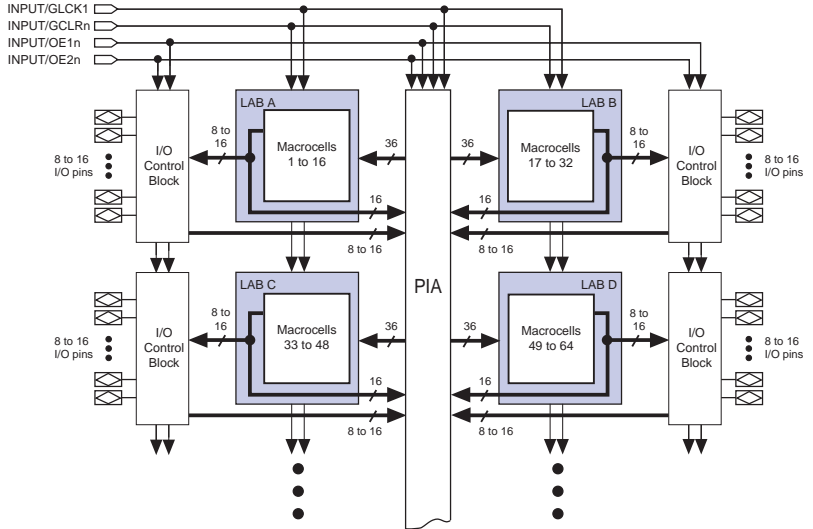
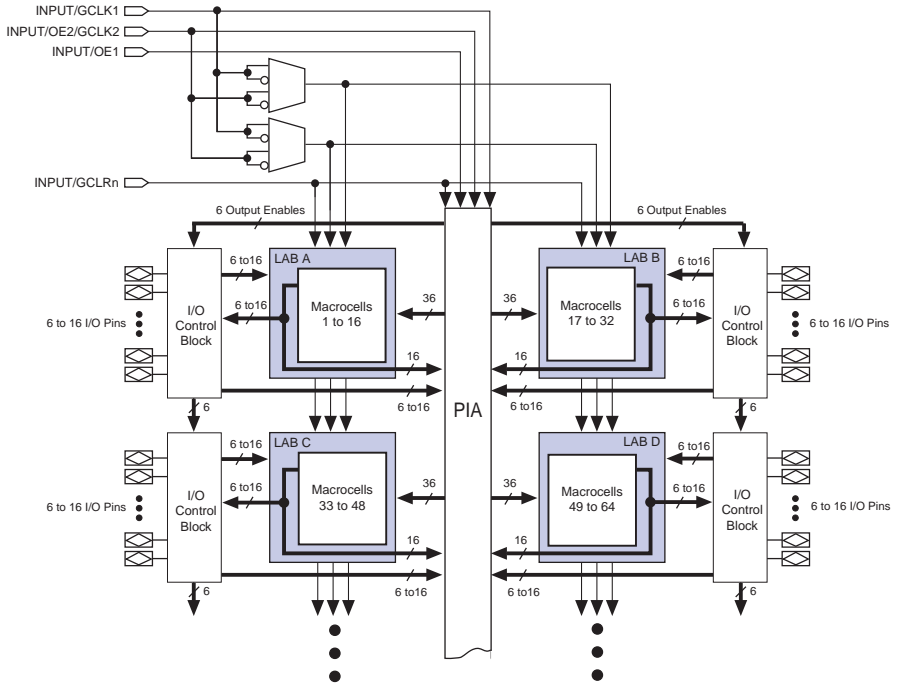


Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

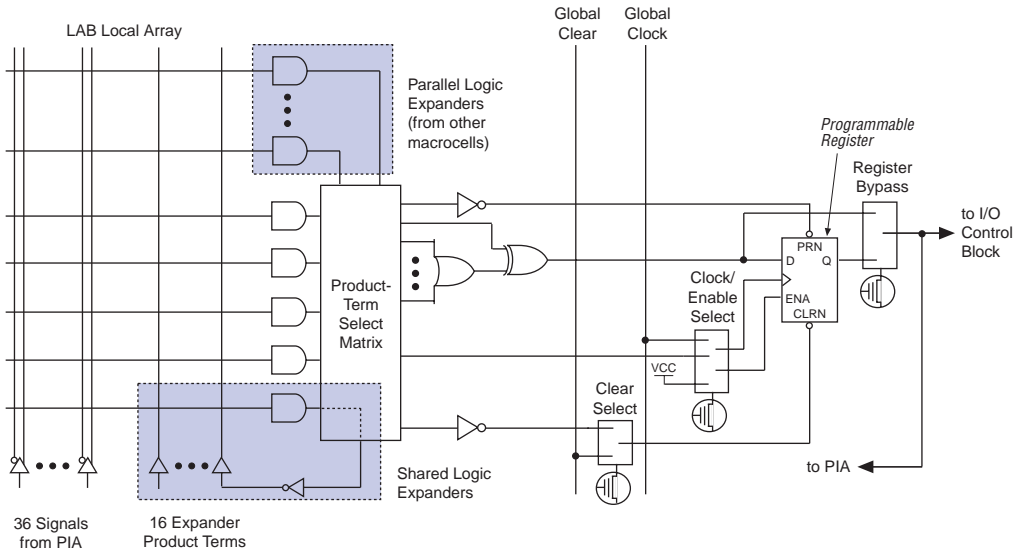
Each LAB is fed by the following signals:

- 36 signals from the programmable interconnect array (PIA) that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

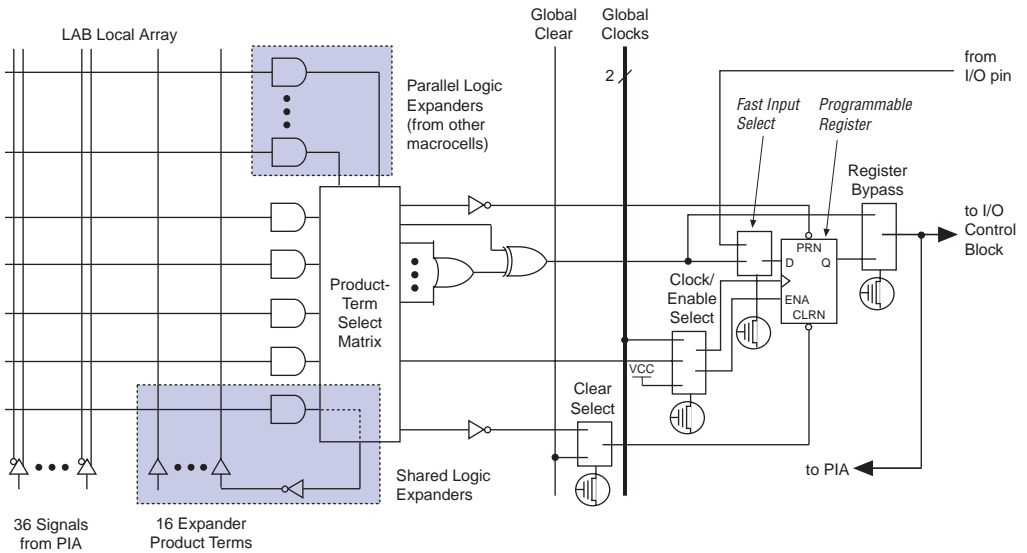
Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7032V, EPM7064, and EPM7096 devices is shown in Figure 3.

Figure 3. EPM7032, EPM7032V, EPM7064 & EPM7096 Device Macrocell



The macrocell of MAX 7000E and MAX 7000S devices is shown in Figure 4.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell

Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7032V, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (3-ns) input setup time.

Expander Product Terms

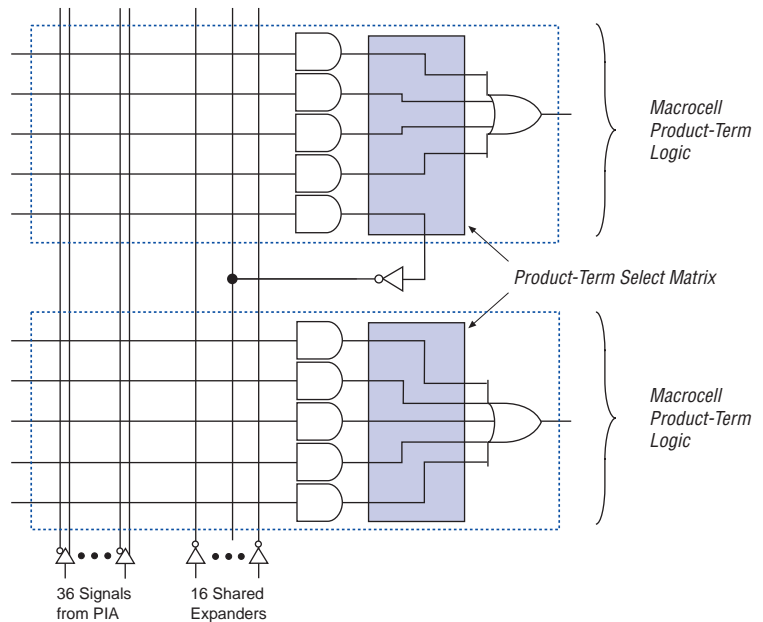
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. [Figure 5](#) shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

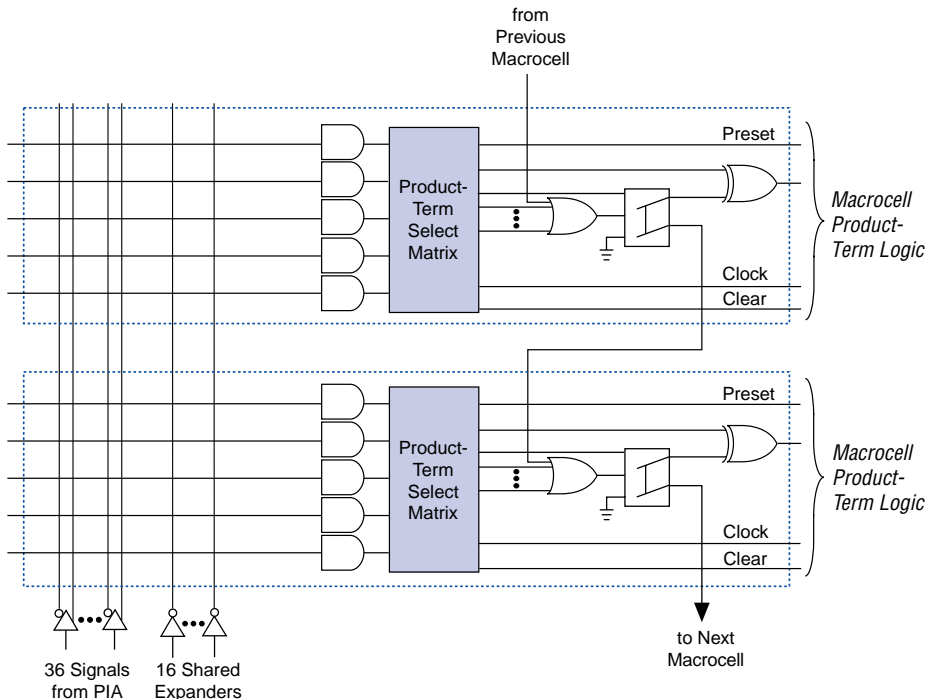
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can allocate up to 3 sets of up to 5 parallel expanders automatically to the macrocells that require additional product terms. Each set of 5 parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. **Figure 6** shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

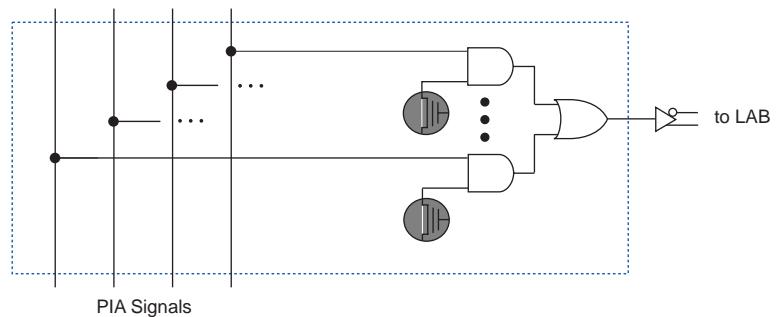
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

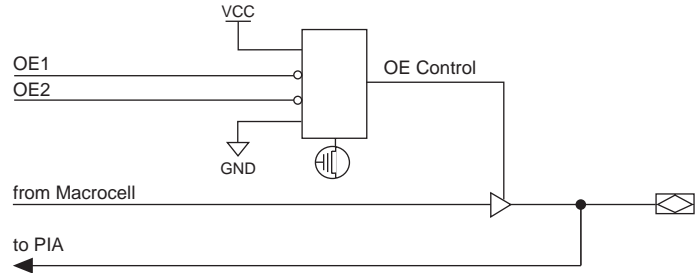
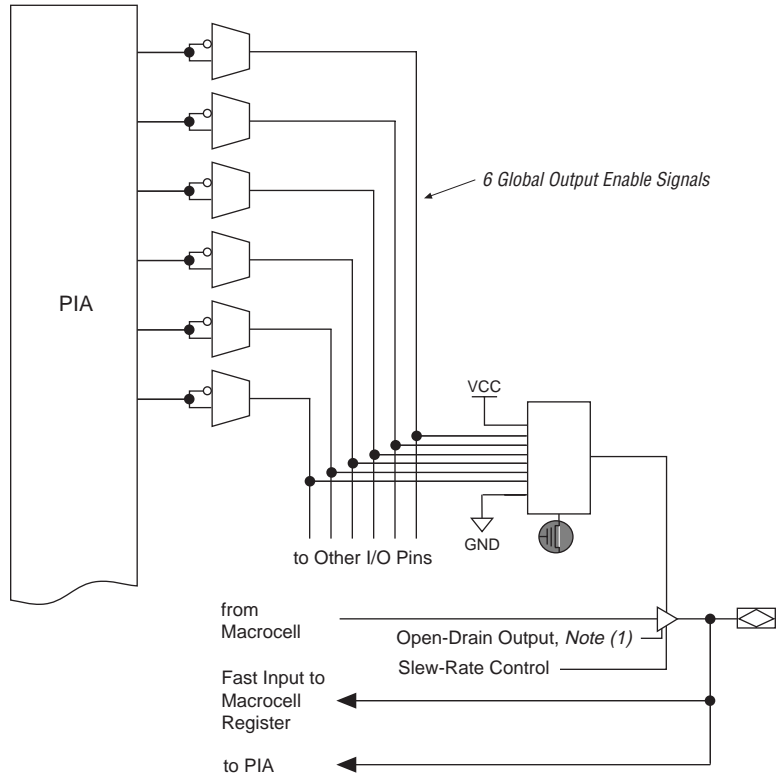
Figure 7. PIA Routing



While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7032V, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 8. I/O Control Block of MAX 7000 Devices**EPM7032, EPM7032V, EPM7064 & EPM7096 Devices****MAX 7000E & MAX 7000S Devices****Note:**

(1) The open-drain output option is available in MAX 7000S devices only.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit test (ICT) equipment, embedded processors, or the Altera BitBlaster or ByteBlaster download cables. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000S devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some ICT platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm are marked with an "F" suffix in the ordering code.

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

Output Configuration

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{EN} , and t_{SEXP} parameters.

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

MAX 7000 devices, except 44-pin devices, support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both low voltage and VCCINT inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1} .

Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on 486- and Pentium-based PCs with the MAX+PLUS II Programmer, an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera Programming Hardware* in the **1998 Data Book**.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers* in the **1998 Data Book**.

IEEE 1149.1 (JTAG) Boundary-Scan Support

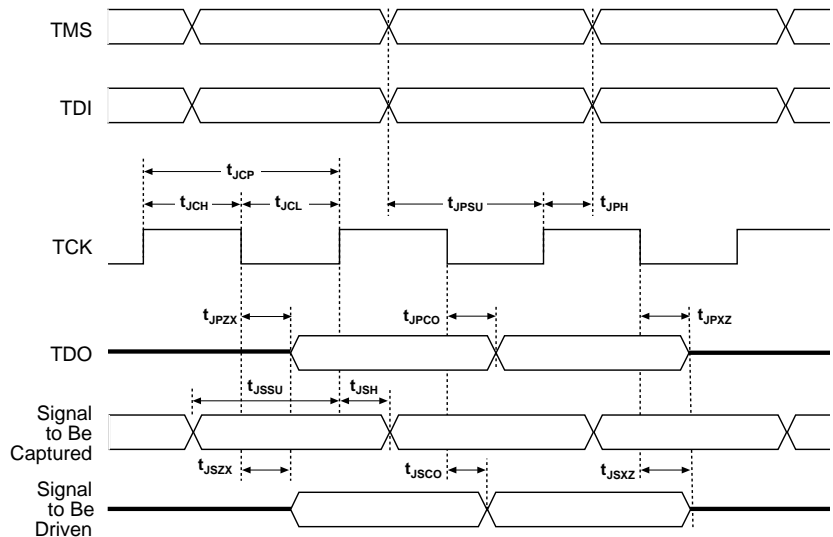
MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. [Table 5](#) describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables starting on [page 45](#) of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

| Table 5. MAX 7000 JTAG Instructions (Part 1 of 2) | | |
|---|--|--|
| JTAG Instruction | Devices | Description |
| SAMPLE/PRELOAD | EPM7128S EPM7160S EPM7192S EPM7256S | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins. |
| EXTEST | EPM7128S EPM7160S EPM7192S EPM7256S | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |

Table 5. MAX 7000 JTAG Instructions (Part 2 of 2)

| JTAG Instruction | Devices | Description |
|------------------|--|---|
| BYPASS | EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation. |
| IDCODE | EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| ISP Instructions | EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S | These instructions are used when programming MAX 7000S devices via the JTAG ports with the BitBlaster or ByteBlaster download cable, or using a Jam File or Serial Vector Format (.svf) file via an embedded processor or test equipment. |

Figure 9 shows the timing requirements for the JTAG signals.

Figure 9. MAX 7000 JTAG Waveforms

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Go to [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information.

Design Security

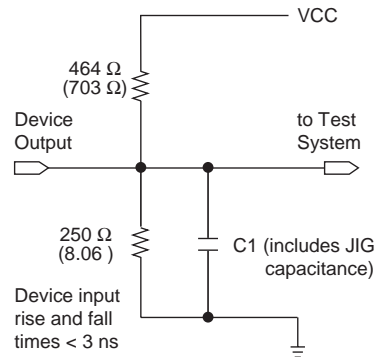
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000 devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 10](#). Test patterns can be used and then erased during early stages of the production flow.

Figure 10. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.



QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. For detailed information and carrier dimensions, refer to the [QFP Carrier & Development Socket Data Sheet](#) in the **1998 Data Book**.

- 1 MAX 7000S devices are not shipped in carriers.

Operating Conditions

The following tables provide information of absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|----------------------------|---|------|-----|------|
| V_{CC} | Supply voltage | With respect to ground, <i>Note (2)</i> | -2.0 | 7.0 | V |
| V_I | DC input voltage | | -2.0 | 7.0 | V |
| I_{OUT} | DC output current, per pin | | -25 | 25 | mA |
| T_{STG} | Storage temperature | No bias | -65 | 150 | °C |
| T_{AMB} | Ambient temperature | Under bias | -65 | 135 | °C |
| T_J | Junction temperature | Ceramic packages, under bias | | 150 | °C |
| | | PQFP and RQFP packages, under bias | | 135 | °C |

MAX 7000 5.0-V Device Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------|---|----------------------------|----------------|----------------|------|
| V_{CCINT} | Supply voltage for internal logic and input buffers | <i>Notes (3), (4)</i> | 4.75 (4.50) | 5.25 (5.50) | V |
| V_{CCIO} | Supply voltage for output drivers, 5.0-V operation | <i>Notes (3), (4)</i> | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | <i>Notes (3), (4), (5)</i> | 3.00 (3.00) | 3.60 (3.60) | V |
| V_{CCISP} | Supply voltage during ISP | <i>Note (6)</i> | 4.75 | 5.25 | V |
| V_I | Input voltage | | 0 | V_{CCINT} | V |
| V_O | Output voltage | | 0 | V_{CCIO} | V |
| T_A | Ambient temperature | For commercial use | 0 | 70 | °C |
| | | For industrial use | -40 | 85 | °C |
| T_J | Junction temperature | For commercial use | 0 | 90 | °C |
| | | For industrial use | -40 | 105 | °C |
| t_R | Input rise time | | | 40 | ns |
| t_F | Input fall time | | | 40 | ns |

MAX 7000 5.0-V Device DC Operating Conditions *Note (7)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|--|--|------------------|-------------------|---------|
| V_{IH} | High-level input voltage | | 2.0 | $V_{CCINT} + 0.3$ | V |
| V_{IL} | Low-level input voltage | | -0.3 | 0.8 | V |
| V_{OH} | 5.0-V high-level TTL output voltage | $I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V, <i>Note (8)</i> | 2.4 | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V, <i>Note (8)</i> | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.0$ V, <i>Note (8)</i> | $V_{CCIO} - 0.2$ | | V |
| V_{OL} | 5.0-V low-level TTL output voltage | $I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V, <i>Note (9)</i> | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V, <i>Note (8)</i> | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.0$ V, <i>Note (9)</i> | | 0.2 | V |
| I_I | Leakage current of dedicated input pins | $V_I = V_{CC}$ or ground | -10 | 10 | μ A |
| I_{OZ} | I/O pin tri-state output off-state current | $V_O = V_{CC}$ or ground, <i>Note (10)</i> | -40 | 40 | μ A |

MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (11)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-----------------------|--------------------------------|-----|-----|------|
| C_{IN} | Input pin capacitance | $V_{IN} = 0$ V, $f = 1.0$ MHz | | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT} = 0$ V, $f = 1.0$ MHz | | 12 | pF |

MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (11)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-----------------------|--------------------------------|-----|-----|------|
| C_{IN} | Input pin capacitance | $V_{IN} = 0$ V, $f = 1.0$ MHz | | 15 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT} = 0$ V, $f = 1.0$ MHz | | 15 | pF |

MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (11)*

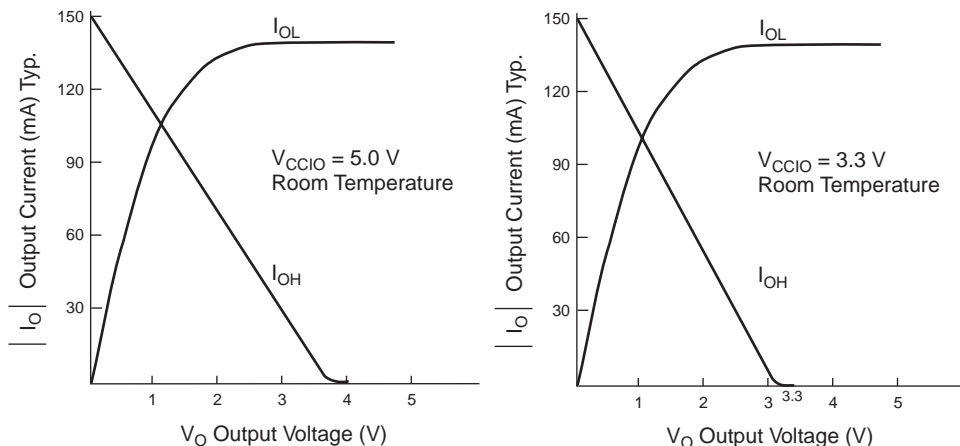
| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------------|--------------------------------|-----|-----|------|
| C_{IN} | Dedicated input pin capacitance | $V_{IN} = 0$ V, $f = 1.0$ MHz | | 10 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT} = 0$ V, $f = 1.0$ MHz | | 10 | pF |

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet* in the **1998 Data Book**.
- (2) Minimum DC input is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) V_{CC} must rise monotonically.
- (5) 3.3 -V I/O operation is not available for 44-pin packages.
- (6) The V_{CCISF} parameter applies only to MAX 7000S devices.
- (7) These values are specified under the “MAX 7000 5.0 V Device Recommended Operating Conditions” on page 21.
- (8) The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (9) The I_{OL} parameter refers to low-level TTL or CMOS output current.
- (10) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically -60 μ A.
- (11) Capacitance is measured at 25° C and is sample-tested only. The $OE1$ pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices



3.3-V EPM7032V Devices

EPM7032V devices are high-performance MAX 7000 devices that meet the low power and low voltage requirements of 3.3-V applications ranging from notebook computers to battery-operated, hand-held equipment. EPM7032V devices provide in-system speeds of up to 90.9 MHz and propagation delays of 12 ns. The devices are available in 44-pin reprogrammable PLCC or TQFP packages and can accommodate designs with up to 36 inputs and 32 outputs.

Power Management

The 3.3-V operation of EPM7032V devices offer power savings of 30% to 50% over the 5.0-V operation of EPM7032 devices. Power-saving features of EPM7032V devices include a power-down mode and a programmable speed/power control as specified for non-3.3-V MAX 7000 devices.

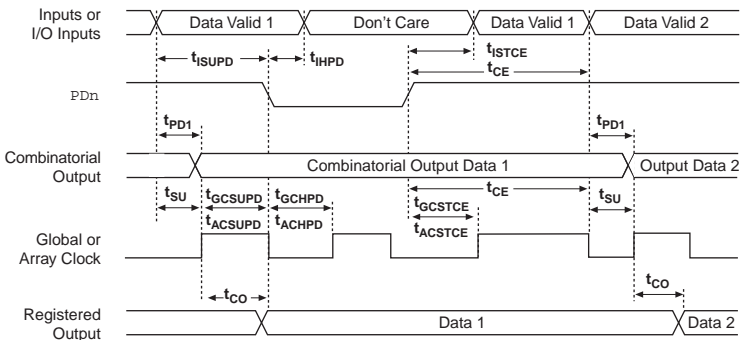
Power-Down Mode

EPM7032V devices provide a unique power-down mode that allows the device to consume near-zero power (typically 50 μ A). The power-down mode is controlled externally by the dedicated power-down pin (PDn). When PDn is asserted (active low), the power-down sequence latches all input pins, internal logic, and output pins of the EPM7032V device, preserving their present state. Output pins maintain their present low, high, or tri-state value while in power-down mode.

Once in power-down mode, any or all of the inputs, including clocks, can be toggled without affecting the state of the device. Because internal latches are used to ensure that the proper state exists during power-down mode, the external inputs and clocks must meet certain setup and hold time requirements. See Figure 12 and the “Power-Down Timing Parameters” and “Chip-Enable Timing Parameters” tables on page 40 of this data sheet.

Figure 12. Power-Down Mode Switching Waveforms

The switching waveforms for EPM7032V devices are identical to those of 5.0-V EPM7032 devices in all modes, except for the additional power-down mode shown here. t_R and $t_F < 3$ ns. Inputs are driven at 3.0 V for a logic high and 0.0 V for a logic low. All timing characteristics are measured at 1.5 V.



When the $\overline{\text{PDn}}$ signal is deasserted, the device is enabled and the combinatorial outputs respond to the present input conditions within the specified chip enable delay (t_{CE}). Registered outputs respond to clock transitions within t_{CE} . Clocking the device during the chip enable sequence can cause the data to change inside the chip if a clock transition occurs during certain intervals of the chip enable or chip disable sequences. All clocks should be gated to prevent clock transitions during the clock setup time (t_{GCSUPD} or t_{ACSUPD}) and during the chip enable setup time (t_{GCSTCE} or t_{ACSTCE}), as shown in Figure 12.

All registers in EPM7032V devices provide clock enable control, which makes it easy to disable clocks. If output signals must be frozen in a high-impedance state during power-down, the associated output enable signal must be asserted, the system clock must be removed, and the $\overline{\text{PDn}}$ pin must be asserted. To reactivate the device, the sequence is reversed. For some systems, it may be more appropriate to switch the order of the clock and output enable controls.

All power-down/chip-enable timing parameters are computed from external input or I/O pins, with the macrocell Turbo Bit option turned on, and without the use of parallel expanders. For macrocells in low-power mode (Turbo Bit off), the low-power adder, t_{LPA} , must be added to the power-down/chip enable timing parameters, which include the data paths t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{ACH} , and t_{SEXP} . For macrocells that use shared or parallel expanders, t_{SEXP} or t_{PEXP} must be added. For data or clock paths that use more than one logic array delay, the worst-case data or clock delay must be added to the respective power-down/chip-enable parameters. Actual worst-case timing of data and clock paths can be calculated with the MAX+PLUS II Simulator or Timing Analyzer, or with other industry-standard EDA verification tools.

EPM7032V 3.3-V Device Absolute Maximum Ratings *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------|---|------|-----|------|
| V_{CC} | Supply voltage | With respect to ground, <i>Note (2)</i> | -2.0 | 5.6 | V |
| V_{I} | DC input voltage | | -2.0 | 5.6 | V |
| I_{OUT} | DC output current per pin | | -25 | 25 | mA |
| T_{STG} | Storage temperature | No bias | -65 | 150 | °C |
| T_{AMB} | Ambient temperature | Under bias | -65 | 135 | °C |
| T_{J} | Junction temperature | Under bias | 0 | 135 | °C |

EPM7032V 3.3-V Device Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|-----------------------|--------------------|-----|----------|------|
| V_{CC} | Supply voltage | Note (3) | 3.0 | 3.6 | V |
| V_I | Input voltage | | 0 | V_{CC} | V |
| V_O | Output voltage | | 0 | V_{CC} | V |
| T_A | Operating temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| T_J | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use | –40 | 105 | ° C |
| t_R | Input rise time | | | 40 | ns |
| t_F | Input fall time | | | 40 | ns |

EPM7032V 3.3-V Device DC Operating Conditions Notes (4), (5)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--|--|----------------|-----|----------------|------|
| V_{IH} | High-level input voltage | | 2.0 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Low-level input voltage | | –0.3 | | 0.8 | V |
| V_{OH} | High-level TTL output voltage | $I_{OH} = -0.1$ mA DC, Note (6) | $V_{CC} - 0.2$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 4$ mA DC, Note (7) | | | 0.45 | V |
| I_I | Input leakage current | $V_I = V_{CC}$ or ground | –10 | | 10 | μA |
| I_{OZ} | Tri-state output off-state current | $V_O = V_{CC}$ or ground | –10 | | 10 | μA |
| I_{CC0} | V_{CC} supply current (standby, power-down mode) | Note (8) | | 2 | 150 | μA |
| I_{CC1} | V_{CC} supply current (standby, low-power mode) | $V_I =$ ground, no load, Note (8) | | 10 | 20 | mA |
| I_{CC2} | V_{CC} supply current (active, low-power mode) | $V_I =$ ground, no load, $f = 1.0$ MHz, Note (8) | | 15 | 25 | mA |

EPM7032V 3.3-V Device Capacitance Note (9)

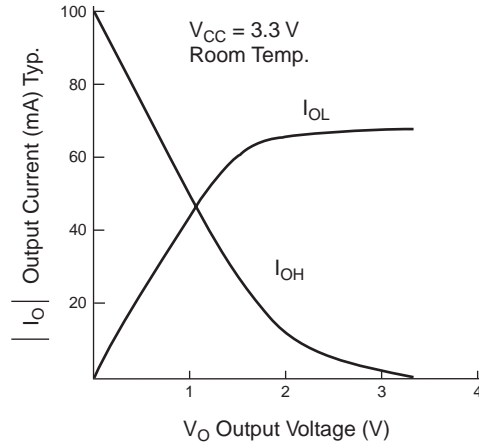
| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-----------------------------|--------------------------------|-----|-----|------|
| C_{IN} | Dedicated input capacitance | $V_{IN} = 0$ V, $f = 1.0$ MHz | | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT} = 0$ V, $f = 1.0$ MHz | | 12 | pF |

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet* in the **1998 Data Book**.
- (2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to $V_{CC} + 2.0$ V for periods shorter than 20 ns under no-load conditions.
- (3) V_{CC} must rise monotonically.
- (4) Typical values are for $T_A = 25^\circ$ C and $V_{CC} = 3.3$ V.
- (5) These values are specified under the “MAX 7000 5.0 V Device Recommended Operating Conditions” on page 21.
- (6) The I_{OH} parameter refers to high-level TTL output current.
- (7) The I_{OL} parameter refers to low-level TTL output current.
- (8) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.
- (9) Capacitance is measured at 25° C and is sample-tested only. The $\odot E1$ pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

Figure 13 shows the typical output drive characteristics of EPM7032V devices.

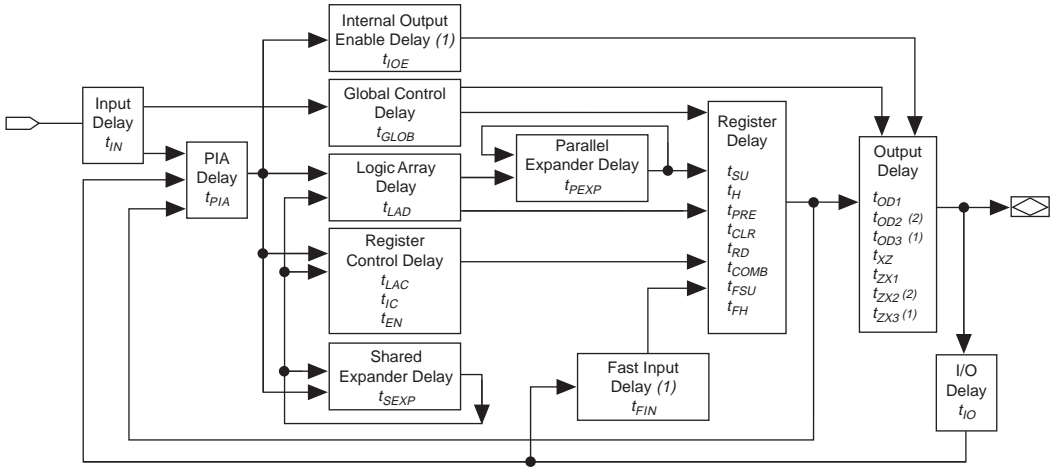
Figure 13. EPM7032V Output Drive Characteristics



Timing Model

MAX 7000 device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 14. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 14. MAX 7000 Timing Model



Notes:

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters.

Figure 15 shows the internal timing relationship of internal and external delay parameters.

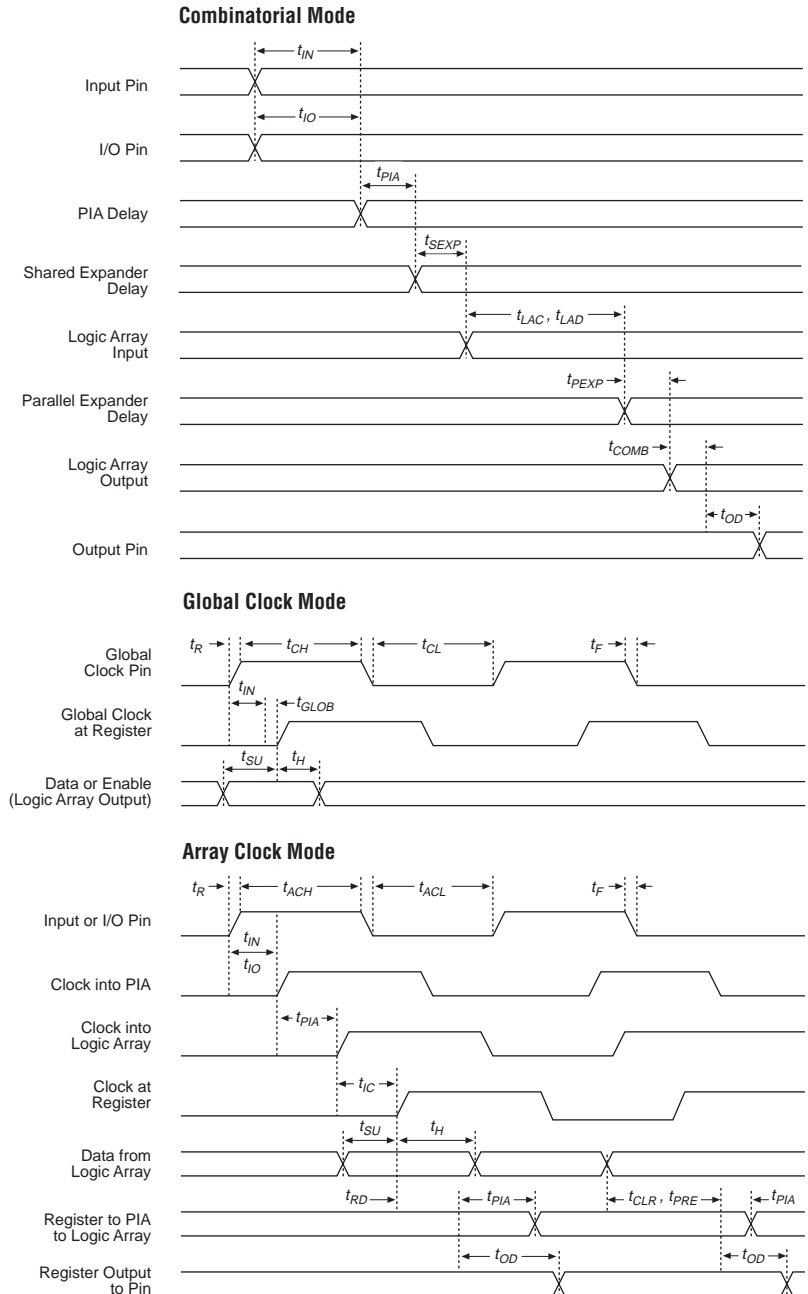
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See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) in this handbook for more information.

Figure 15. Switching Waveforms

t_R & $t_F < 3$ ns.

Inputs are driven at 3 V
for a logic high and 0 V
for a logic low. All timing
characteristics are
measured at 1.5 V.



MAX 7000 AC Operating Conditions *Notes (1), (2)*

| External Timing Parameters | | | Speed Grade | | | | | | |
|----------------------------|---|----------------------|-------------|-----|-------|-----|-------|-----|------|
| | | | -5 | | -6 | | -7 | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Min | Max | Unit |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 5 | | 6 | | 7.5 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 5 | | 6 | | 7.5 | ns |
| t _{SU} | Global clock setup time | | 4 | | 5 | | 6 | | ns |
| t _H | Global clock hold time | | 0 | | 0 | | 0 | | ns |
| t _{FSU} | Global clock setup time of fast input | Note (3) | 2.5 | | 2.5 | | 3 | | ns |
| t _{FH} | Global clock hold time of fast input | Note (3) | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 3.5 | | 4 | | 4.5 | ns |
| t _{CH} | Global clock high time | | 2 | | 2.5 | | 3 | | ns |
| t _{CL} | Global clock low time | | 2 | | 2.5 | | 3 | | ns |
| t _{ASU} | Array clock setup time | | 2 | | 2.5 | | 3 | | ns |
| t _{AH} | Array clock hold time | | 2 | | 2 | | 2 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 5.5 | | 6.5 | | 7.5 | ns |
| t _{ACH} | Array clock high time | | 2.5 | | 3 | | 3 | | ns |
| t _{ACL} | Array clock low time | | 2.5 | | 3 | | 3 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF, Note (4) | 1 | | 1 | | 1 | | ns |
| t _{CNT} | Minimum global clock period | | | 5.6 | | 6.6 | | 8 | ns |
| f _{CNT} | Maximum internal global clock frequency | Note (5) | 178.6 | | 151.5 | | 125 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 5.6 | | 6.6 | | 8 | ns |
| f _{ACNT} | Maximum internal array clock frequency | Note (5) | 178.6 | | 151.5 | | 125 | | MHz |
| f _{MAX} | Maximum clock frequency | Note (6) | 250 | | 200 | | 166.7 | | MHz |

| Internal Timing Parameters | | | Speed Grade | | | | | | |
|----------------------------|--|---------------------------|-------------|-----|-----|-----|-----|-----|------|
| | | | -5 | | -6 | | -7 | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Min | Max | Unit |
| t_{IN} | Input pad and buffer delay | | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{FIN} | Fast input delay | Note (3) | | 0.8 | | 0.8 | | 1 | ns |
| t_{SEXP} | Shared expander delay | | | 3 | | 3.5 | | 4 | ns |
| t_{PEXP} | Parallel expander delay | | | 0.8 | | 0.8 | | 0.8 | ns |
| t_{LAD} | Logic array delay | | | 1.5 | | 2 | | 3 | ns |
| t_{LAC} | Logic control array delay | | | 1.5 | | 2 | | 3 | ns |
| t_{IOE} | Internal output enable delay | Note (3) | | | | | | 2 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 1.5 | | 2 | | 2 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 3.3$ V | $C1 = 35$ pF, Note (7) | | 2.0 | | 2.5 | | 2.5 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF, Note (3) | | 6.5 | | 7 | | 7 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 4 | | 4 | | 4 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 3.3$ V | $C1 = 35$ pF, Note (7) | | 4.5 | | 4.5 | | 4.5 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF, Note (3) | | 9 | | 9 | | 9 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5$ pF | | 4 | | 4 | | 4 | ns |
| t_{SU} | Register setup time | | 2.5 | | 3 | | 3 | | ns |
| t_H | Register hold time | | 1.5 | | 1.5 | | 2 | | ns |
| t_{FSU} | Register setup time of fast input | Note (3) | 2.5 | | 2.5 | | 3 | | ns |
| t_{FH} | Register hold time of fast input | Note (3) | 0.5 | | 0.5 | | 0.5 | | ns |
| t_{RD} | Register delay | | | 0.8 | | 0.8 | | 1 | ns |
| t_{COMB} | Combinatorial delay | | | 0.8 | | 0.8 | | 1 | ns |
| t_{IC} | Array clock delay | | | 2 | | 2.5 | | 3 | ns |
| t_{EN} | Register enable time | | | 1.5 | | 2 | | 3 | ns |
| t_{GLOB} | Global control delay | | | 0.8 | | 0.8 | | 1 | ns |
| t_{PRE} | Register preset time | | | 2 | | 2 | | 2 | ns |
| t_{CLR} | Register clear time | | | 2 | | 2 | | 2 | ns |
| t_{PIA} | PIA delay | | | 0.8 | | 0.8 | | 1 | ns |
| t_{LPA} | Low-power adder | Note (8) | | 8 | | 10 | | 10 | ns |

| External Timing Parameters | | | Speed Grade | | | | |
|----------------------------|---|----------------------|-------------------------------------|-----|-----------------------------------|-----|------|
| | | | MAX 7000E (-10P) MAX 7000S (-10) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Unit |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 10 | | 10 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 10 | | 10 | ns |
| t _{SU} | Global clock setup time | | 7 | | 8 | | ns |
| t _H | Global clock hold time | | 0 | | 0 | | ns |
| t _{FSU} | Global clock setup time of fast input | Note (3) | 3 | | 3 | | ns |
| t _{FH} | Global clock hold time of fast input | Note (3) | 0.5 | | 0.5 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 5 | | 5 | ns |
| t _{CH} | Global clock high time | | 4 | | 4 | | ns |
| t _{CL} | Global clock low time | | 4 | | 4 | | ns |
| t _{ASU} | Array clock setup time | | 2 | | 3 | | ns |
| t _{AH} | Array clock hold time | | 3 | | 3 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 10 | | 10 | ns |
| t _{ACH} | Array clock high time | | 4 | | 4 | | ns |
| t _{ACL} | Array clock low time | | 4 | | 4 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF, Note (4) | 1 | | 1 | | ns |
| t _{CNT} | Minimum global clock period | | | 10 | | 10 | ns |
| f _{CNT} | Maximum internal global clock frequency | Note (5) | 100 | | 100 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 10 | | 10 | ns |
| f _{ACNT} | Maximum internal array clock frequency | Note (5) | 100 | | 100 | | MHz |
| f _{MAX} | Maximum clock frequency | Note (6) | 125 | | 125 | | MHz |

| Internal Timing Parameters | | | Speed Grade | | | | |
|----------------------------|---|------------------------|-------------------------------------|-----|-----------------------------------|-----|------|
| | | | MAX 7000E (-10P) MAX 7000S (-10) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Unit |
| t_{IN} | Input pad and buffer delay | | | 0.5 | | 1 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 0.5 | | 1 | ns |
| t_{FIN} | Fast input delay | Note (3) | | 1 | | 1 | ns |
| t_{SEXP} | Shared expander delay | | | 5 | | 5 | ns |
| t_{PEXP} | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| t_{LAD} | Logic array delay | | | 5 | | 5 | ns |
| t_{LAC} | Logic control array delay | | | 5 | | 5 | ns |
| t_{IOE} | Internal output enable delay | Note (3) | | 2 | | 2 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 1.5 | | 2 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V | $C1 = 35$ pF, Note (7) | | 2 | | 2.5 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF, Note (3) | | 5.5 | | 6 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 5 | | 5 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V | $C1 = 35$ pF, Note (7) | | 5.5 | | 5.5 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF, Note (3) | | 9 | | 9 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5$ pF | | 5 | | 5 | ns |
| t_{SU} | Register setup time | | 2 | | 3 | | ns |
| t_H | Register hold time | | 3 | | 3 | | ns |
| t_{FSU} | Register setup time of fast input | Note (3) | 3 | | 3 | | ns |
| t_{FH} | Register hold time of fast input | Note (3) | 0.5 | | 0.5 | | ns |
| t_{RD} | Register delay | | | 2 | | 1 | ns |
| t_{COMB} | Combinatorial delay | | | 2 | | 1 | ns |
| t_{IC} | Array clock delay | | | 5 | | 5 | ns |
| t_{EN} | Register enable time | | | 5 | | 5 | ns |
| t_{GLOB} | Global control delay | | | 1 | | 1 | ns |
| t_{PRE} | Register preset time | | | 3 | | 3 | ns |
| t_{CLR} | Register clear time | | | 3 | | 3 | ns |
| t_{PIA} | PIA delay | | | 1 | | 1 | ns |
| t_{LPA} | Low-power adder | Note (8) | | 11 | | 11 | ns |

| External Timing Parameters | | | Speed Grade | | | | |
|----------------------------|---|----------------------|------------------|-----|-----------------------------------|-----|------|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Unit |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 12 | | 12 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 12 | | 12 | ns |
| t _{SU} | Global clock setup time | | 7 | | 10 | | ns |
| t _H | Global clock hold time | | 0 | | 0 | | ns |
| t _{FSU} | Global clock setup time of fast input | Note (3) | 3 | | 3 | | ns |
| t _{FH} | Global clock hold time of fast input | Note (3) | 0 | | 0 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 6 | | 6 | ns |
| t _{CH} | Global clock high time | | 4 | | 4 | | ns |
| t _{CL} | Global clock low time | | 4 | | 4 | | ns |
| t _{ASU} | Array clock setup time | | 3 | | 4 | | ns |
| t _{AH} | Array clock hold time | | 4 | | 4 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 12 | | 12 | ns |
| t _{ACH} | Array clock high time | | 5 | | 5 | | ns |
| t _{ACL} | Array clock low time | | 5 | | 5 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF, Note (4) | 1 | | 1 | | ns |
| t _{CNT} | Minimum global clock period | | | 11 | | 11 | ns |
| f _{CNT} | Maximum internal global clock frequency | Note (8) | 90.9 | | 90.9 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 11 | | 11 | ns |
| f _{ACNT} | Maximum internal array clock frequency | Note (8) | 90.9 | | 90.9 | | MHz |
| f _{MAX} | Maximum clock frequency | Note (6) | 125 | | 125 | | MHz |

| Internal Timing Parameters | | | Speed Grade | | | | |
|----------------------------|---|--------------------------------|------------------|-----|-----------------------------------|-----|------|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Unit |
| t_{IN} | Input pad and buffer delay | | | 1 | | 2 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 1 | | 2 | ns |
| t_{FIN} | Fast input delay | Note (3) | | 1 | | 1 | ns |
| t_{SEXP} | Shared expander delay | | | 7 | | 7 | ns |
| t_{PEXP} | Parallel expander delay | | | 1 | | 1 | ns |
| t_{LAD} | Logic array delay | | | 7 | | 5 | ns |
| t_{LAC} | Logic control array delay | | | 5 | | 5 | ns |
| t_{IOE} | Internal output enable delay | Note (3) | | 2 | | 2 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$ | $C1 = 35\text{ pF}$ | | 1 | | 3 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$ | $C1 = 35\text{ pF}$, Note (7) | | 2 | | 4 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V | $C1 = 35\text{ pF}$, Note (3) | | 5 | | 7 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$ | $C1 = 35\text{ pF}$ | | 6 | | 6 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$ | $C1 = 35\text{ pF}$, Note (7) | | 7 | | 7 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V | $C1 = 35\text{ pF}$, Note (3) | | 10 | | 10 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5\text{ pF}$ | | 6 | | 6 | ns |
| t_{SU} | Register setup time | | 1 | | 4 | | ns |
| t_H | Register hold time | | 6 | | 4 | | ns |
| t_{FSU} | Register setup time of fast input | Note (3) | 4 | | 2 | | ns |
| t_{FH} | Register hold time of fast input | Note (3) | 0 | | 2 | | ns |
| t_{RD} | Register delay | | | 2 | | 1 | ns |
| t_{COMB} | Combinatorial delay | | | 2 | | 1 | ns |
| t_{IC} | Array clock delay | | | 5 | | 5 | ns |
| t_{EN} | Register enable time | | | 7 | | 5 | ns |
| t_{GLOB} | Global control delay | | | 2 | | 0 | ns |
| t_{PRE} | Register preset time | | | 4 | | 3 | ns |
| t_{CLR} | Register clear time | | | 4 | | 3 | ns |
| t_{PIA} | PIA delay | | | 1 | | 1 | ns |
| t_{LPA} | Low-power adder | Note (8) | | 12 | | 12 | ns |

| External Timing Parameters | | | Speed Grade | | | | | | |
|----------------------------|---|----------------------|-------------|-----|------|-----|------|-----|------|
| | | | -15 | | -15T | | -20 | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Min | Max | Unit |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 15 | | 15 | | 20 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 15 | | 15 | | 20 | ns |
| t _{SU} | Global clock setup time | | 11 | | 11 | | 12 | | ns |
| t _H | Global clock hold time | | 0 | | 0 | | 0 | | ns |
| t _{FSU} | Global clock setup time of fast input | Note (3) | 3 | | – | | 5 | | ns |
| t _{FH} | Global clock hold time of fast input | Note (3) | 0 | | – | | 0 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 8 | | 8 | | 12 | ns |
| t _{CH} | Global clock high time | | 5 | | 6 | | 6 | | ns |
| t _{CL} | Global clock low time | | 5 | | 6 | | 6 | | ns |
| t _{ASU} | Array clock setup time | | 4 | | 4 | | 5 | | ns |
| t _{AH} | Array clock hold time | | 4 | | 4 | | 5 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 15 | | 15 | | 20 | ns |
| t _{ACH} | Array clock high time | | 6 | | 6.5 | | 8 | | ns |
| t _{ACL} | Array clock low time | | 6 | | 6.5 | | 8 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF, Note (4) | 1 | | 1 | | 1 | | ns |
| t _{CNT} | Minimum global clock period | | | 13 | | 13 | | 16 | ns |
| f _{CNT} | Maximum internal global clock frequency | Note (5) | 76.9 | | 76.9 | | 62.5 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 13 | | 13 | | 16 | ns |
| f _{ACNT} | Maximum internal array clock frequency | Note (5) | 76.9 | | 76.9 | | 62.5 | | MHz |
| f _{MAX} | Maximum clock frequency | Note (6) | 100 | | 83.3 | | 83.3 | | MHz |

| Internal Timing Parameters | | | Speed Grade | | | | | | |
|----------------------------|---|---|-------------|-----|------|-----|-----|-----|------|
| | | | -15 | | -15T | | -20 | | |
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Min | Max | Unit |
| t_{IN} | Input pad and buffer delay | | | 2 | | 2 | | 3 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 2 | | 2 | | 3 | ns |
| t_{FIN} | Fast input delay | Note (3) | | 2 | | — | | 4 | ns |
| t_{SEXP} | Shared expander delay | | | 8 | | 10 | | 9 | ns |
| t_{PEXP} | Parallel expander delay | | | 1 | | 1 | | 2 | ns |
| t_{LAD} | Logic array delay | | | 6 | | 6 | | 8 | ns |
| t_{LAC} | Logic control array delay | | | 6 | | 6 | | 8 | ns |
| t_{IOE} | Internal output enable delay | Note (3) | | 3 | | — | | 4 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$ | $C1 = 35\text{ pF}$ | | 4 | | 4 | | 5 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$ | $C1 = 35\text{ pF}$, Note (7) | | 5 | | — | | 6 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V | $C1 = 35\text{ pF}$, Notes (3), (7) | | 8 | | — | | 9 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$ | $C1 = 35\text{ pF}$ | | 6 | | 6 | | 10 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$ | $C1 = 35\text{ pF}$, Note (7) | | 7 | | — | | 11 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V | $C1 = 35\text{ pF}$, Notes (3), (7) | | 10 | | — | | 14 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5\text{ pF}$ | | 6 | | 6 | | 10 | ns |
| t_{SU} | Register setup time | | 4 | | 4 | | 4 | | ns |
| t_H | Register hold time | | 4 | | 4 | | 5 | | ns |
| t_{FSU} | Register setup time of fast input | Note (3) | 2 | | — | | 4 | | ns |
| t_{FH} | Register hold time of fast input | Note (3) | 2 | | — | | 3 | | ns |
| t_{RD} | Register delay | | | 1 | | 1 | | 1 | ns |
| t_{COMB} | Combinatorial delay | | | 1 | | 1 | | 1 | ns |
| t_{IC} | Array clock delay | | | 6 | | 6 | | 8 | ns |
| t_{EN} | Register enable time | | | 6 | | 6 | | 8 | ns |
| t_{GLOB} | Global control delay | | | 1 | | 1 | | 3 | ns |
| t_{PRE} | Register preset time | | | 4 | | 4 | | 4 | ns |
| t_{CLR} | Register clear time | | | 4 | | 4 | | 4 | ns |
| t_{PIA} | PIA delay | | | 2 | | 2 | | 3 | ns |
| t_{LPA} | Low-power adder | Note (8) | | 13 | | 15 | | 15 | ns |

Notes to tables:

- (1) These values are specified under the “MAX 7000 5.0 V Device Recommended Operating Conditions” on page 21.
- (2) Timing parameters for some devices are preliminary. See Table 2 on page 3 of this data sheet for preliminary speed grades and Table 4 on page 5 for preliminary packages.
- (3) This parameter applies only to MAX 7000E and MAX 7000S devices.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The f_{MAX} values represent the highest frequency for pipelined data.
- (7) Operating conditions: $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{EN} , and t_{SEXP} parameters for macrocells running in the low-power mode.

EPM7032V AC Operating Conditions *Note (1)*

| External Timing Parameters | | | EPM7032V-12 | | EPM7032V-15 | | EPM7032V-20 | | |
|-----------------------------------|---|---|-------------|------------|-------------|------------|-------------|------------|-------------|
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Min | Max | Unit |
| t_{PD1} | Input to non-registered output | $C1 = 35 \text{ pF}$ | | 12 | | 15 | | 20 | ns |
| t_{PD2} | I/O input to non-registered output | $C1 = 35 \text{ pF}$ | | 12 | | 15 | | 20 | ns |
| t_{SU} | Global clock setup time | | 10 | | 11 | | 12 | | ns |
| t_{H} | Global clock hold time | | 0 | | 0 | | 0 | | ns |
| t_{CO1} | Global clock to output delay | $C1 = 35 \text{ pF}$ | | 7 | | 8 | | 12 | ns |
| t_{CH} | Global clock high time | | 4 | | 5 | | 6 | | ns |
| t_{CL} | Global clock low time | | 4 | | 5 | | 6 | | ns |
| t_{ASU} | Array clock setup time | | 4 | | 4 | | 5 | | ns |
| t_{AH} | Array clock hold time | | 4 | | 4 | | 5 | | ns |
| t_{ACO1} | Array clock to output delay | $C1 = 35 \text{ pF}$ | | 12 | | 15 | | 20 | ns |
| t_{ACH} | Array clock high time | | 5 | | 6 | | 8 | | ns |
| t_{ACL} | Array clock low time | | 5 | | 6 | | 8 | | ns |
| t_{ODH} | Output data hold time after clock | $C1 = 35 \text{ pF}$, <i>Note (2)</i> | 1 | | 1 | | 1 | | ns |
| t_{CNT} | Minimum global clock period | | | 11 | | 13 | | 16 | ns |
| f_{CNT} | Maximum internal global clock frequency | <i>Note (3)</i> | 90.9 | | 76.9 | | 62.5 | | MHz |
| t_{ACNT} | Minimum array clock period | | | 11 | | 13 | | 16 | ns |
| f_{ACNT} | Maximum internal array clock frequency | <i>Note (3)</i> | 90.9 | | 76.9 | | 62.5 | | MHz |
| f_{MAX} | Maximum clock frequency | <i>Note (4)</i> | 125 | | 100 | | 83.3 | | MHz |

EPM7032V AC Operating Conditions *Note (1)*

| Internal Timing Parameters | | | EPM7032V-12 | | EPM7032V-15 | | EPM7032V-20 | | |
|-----------------------------------|--------------------------------|-------------------|-------------|------------|-------------|------------|-------------|------------|-------------|
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Min | Max | Unit |
| t_{IN} | Input pad and buffer delay | | | 3 | | 2 | | 3 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 3 | | 2 | | 3 | ns |
| t_{SEXP} | Shared expander delay | | | 7 | | 8 | | 9 | ns |
| t_{PEXP} | Parallel expander delay | | | 1 | | 1 | | 2 | ns |
| t_{LAD} | Logic array delay | | | 4 | | 6 | | 8 | ns |
| t_{LAC} | Logic control array delay | | | 4 | | 6 | | 8 | ns |
| t_{OD} | Output buffer and pad delay | C1 = 35 pF | | 3 | | 4 | | 5 | ns |
| t_{ZX} | Output buffer enable delay | C1 = 35 pF | | 6 | | 6 | | 9 | ns |
| t_{XZ} | Output buffer disable delay | C1 = 5 pF | | 6 | | 6 | | 9 | ns |
| t_{SU} | Register setup time | | 5 | | 4 | | 4 | | ns |
| t_H | Register hold time | | 4 | | 4 | | 5 | | ns |
| t_{RD} | Register delay | | | 1 | | 1 | | 1 | ns |
| t_{COMB} | Combinatorial delay | | | 1 | | 1 | | 1 | ns |
| t_{IC} | Array clock delay | | | 4 | | 6 | | 8 | ns |
| t_{EN} | Register enable time | | | 4 | | 6 | | 8 | ns |
| t_{GLOB} | Global control delay | | | 0 | | 1 | | 3 | ns |
| t_{PRE} | Register preset time | | | 3 | | 4 | | 4 | ns |
| t_{CLR} | Register clear time | | | 3 | | 4 | | 4 | ns |
| t_{PIA} | PIA delay | | | 1 | | 2 | | 3 | ns |
| t_{LPA} | Low-power adder | <i>Note (5)</i> | | 15 | | 17 | | 20 | ns |

Notes to tables:

- (1) These values are specified under the “MAX 7000 3.3 V Device Recommended Operating Conditions” on page 26.
- (2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.
- (4) The f_{MAX} values represent the highest frequency for pipelined data.
- (5) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

MAX 7000 3.3-V Device Power-Down/Chip-Enable Timing Parameters

| Power-Down Timing Parameters | | EPM7032V-12 | | EPM7032V-15 | | EPM7032V-20 | | |
|-------------------------------------|---|-------------|-----|-------------|-----|-------------|-----|------|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit |
| t_{ISUPD} | Input or I/O input setup time before power down | 30 | | 30 | | 35 | | ns |
| t_{IHPD} | Input or I/O input hold time after power down | 0 | | 0 | | 0 | | ns |
| t_{GCSUPD} | Global clock setup time before power down | 20 | | 20 | | 25 | | ns |
| t_{GCHPD} | Global clock hold time after power down | 0 | | 0 | | 0 | | ns |
| t_{ACSupD} | Array clock setup time before power down | 30 | | 30 | | 35 | | ns |
| t_{ACHPD} | Array clock hold time after power down | 0 | | 0 | | 0 | | ns |
| t_{HPD} | Minimum high pulse width of power-down pin | 800 | | 800 | | 900 | | ns |
| t_{LPD} | Minimum low pulse width of power-down pin | 800 | | 800 | | 900 | | ns |
| t_{PDOWN} | Power down delay | | 800 | | 800 | | 900 | ns |

| Chip-Enable Timing Parameters | | EPM7032V-12 | | EPM7032V-15 | | EPM7032V-20 | | |
|--------------------------------------|---|-------------|-----|-------------|-----|-------------|-----|------|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit |
| t_{ISTCE} | Input or I/O input stable after chip enable | | 60 | | 60 | | 70 | ns |
| t_{GCSTCE} | Global clock stable after chip enable | | 60 | | 60 | | 70 | ns |
| t_{ACSTCE} | Array clock stable after chip enable | | 60 | | 60 | | 70 | ns |
| t_{CE} | Data stable after chip enable | | 700 | | 700 | | 800 | ns |

Power Consumption

Supply power (P) versus frequency (f_{MAX} in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#) in the **1998 Data Book**.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times \log_{LC}$$

The parameters in this equation are shown below:

- MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
 MC_{DEV} = Number of macrocells in the device
 MC_{USED} = Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt)
 f_{MAX} = Highest clock frequency to the device
 tog_{LC} = Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C = Constants, shown in Table 6

Table 6. MAX 7000 I_{CC} Equation Constants

| Device | A | B | C |
|---------------------------|------|------|-------|
| EPM7032 | 1.87 | 0.52 | 0.144 |
| EPM7032V | 0.83 | 0.40 | 0.048 |
| EPM7064 | 1.63 | 0.74 | 0.144 |
| EPM7096 | 1.63 | 0.74 | 0.144 |
| EPM7128E | 1.17 | 0.54 | 0.096 |
| EPM7160E | 1.17 | 0.54 | 0.096 |
| EPM7192E | 1.17 | 0.54 | 0.096 |
| EPM7256E | 1.17 | 0.54 | 0.096 |
| EPM7032S, <i>Note (1)</i> | 0.93 | 0.40 | 0.040 |
| EPM7064S, <i>Note (1)</i> | 0.93 | 0.40 | 0.040 |
| EPM7128S, <i>Note (1)</i> | 0.93 | 0.40 | 0.040 |
| EPM7160S, <i>Note (1)</i> | 0.93 | 0.40 | 0.040 |
| EPM7192S, <i>Note (1)</i> | 0.93 | 0.40 | 0.040 |
| EPM7256S, <i>Note (1)</i> | 0.93 | 0.40 | 0.040 |

Note:

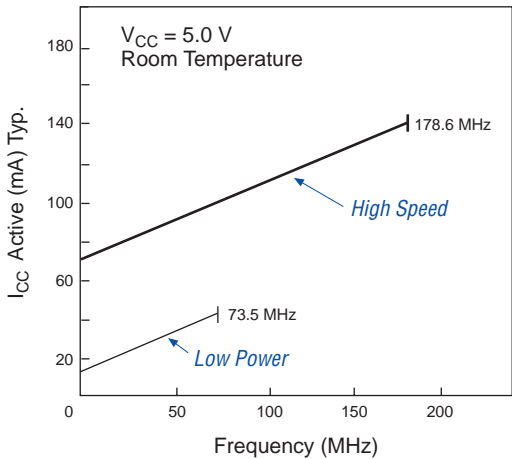
(1) Values for these devices are preliminary.

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

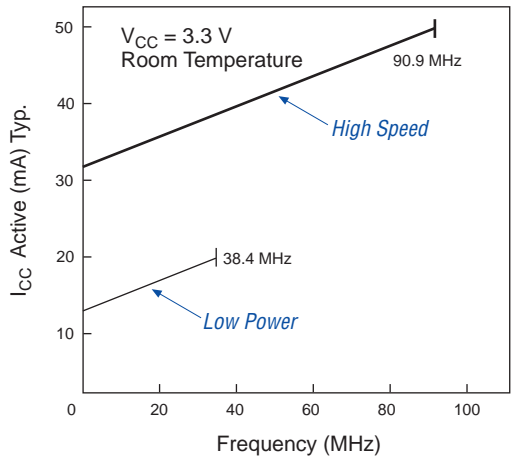
Figure 16 shows typical supply current versus frequency for MAX 7000 devices.

Figure 16. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

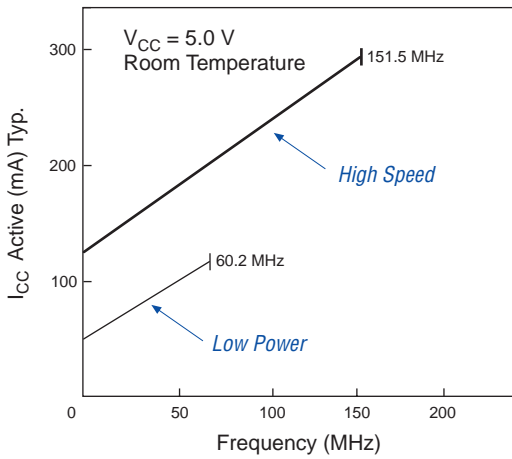
EPM7032



EPM7032V



EPM7064



EPM7096

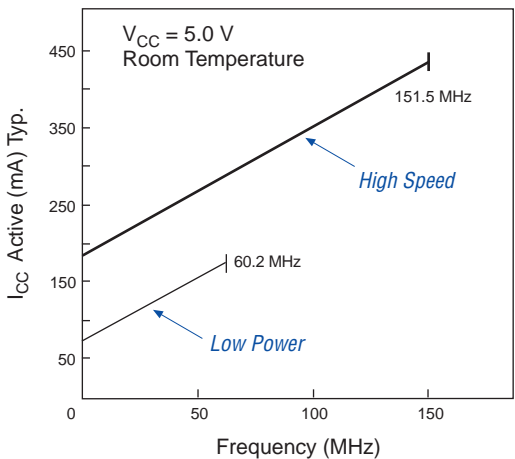
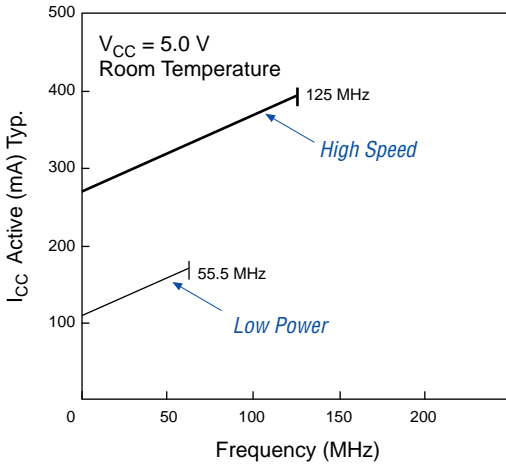
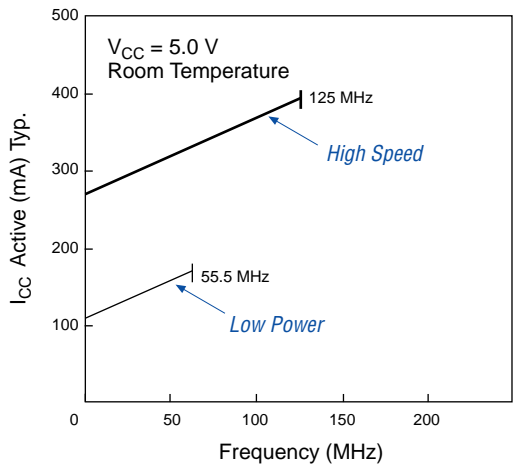


Figure 16. I_{CC} vs. Frequency for MAX 7000 Devices (Part 2 of 2)

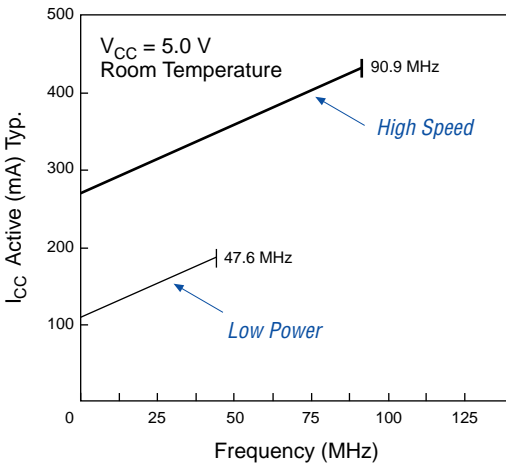
EPM7128E



EPM7160E



EPM7192E



EPM7256E

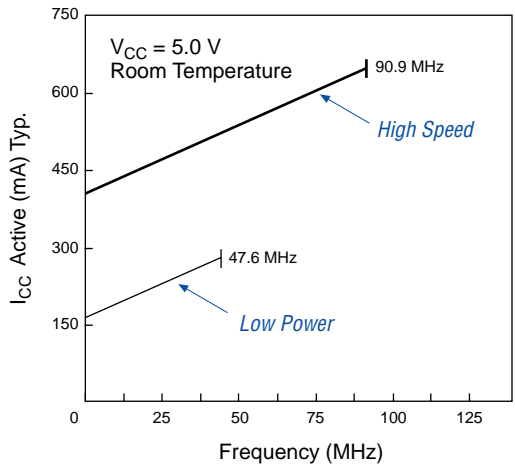
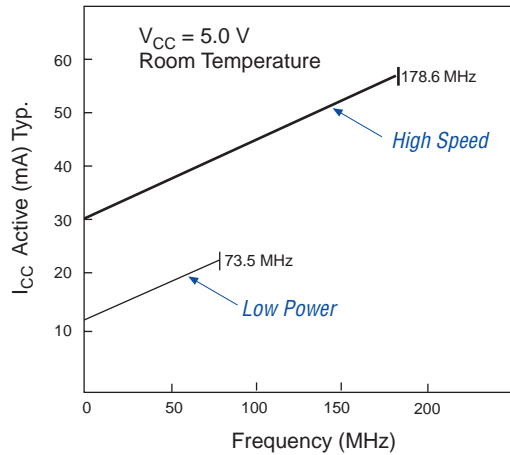


Figure 17 shows typical supply current versus frequency for MAX 7000S devices.

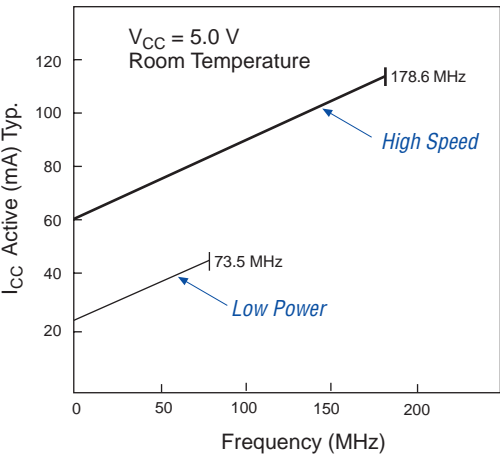
Figure 17. I_{CC} vs. Frequency for MAX 7000S Devices (Part 1 of 2)

Information on MAX 7000S devices is preliminary.

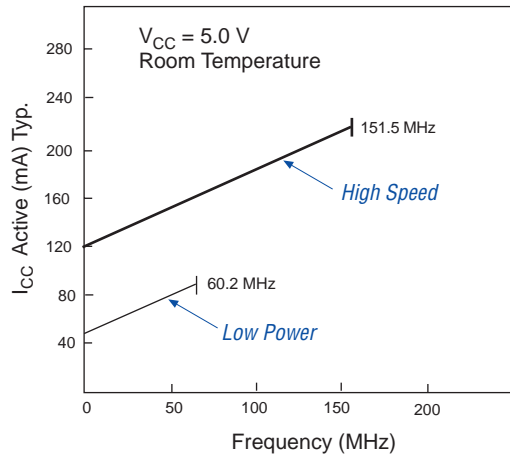
EPM7032S



EPM7064S



EPM7128S



EPM7160S

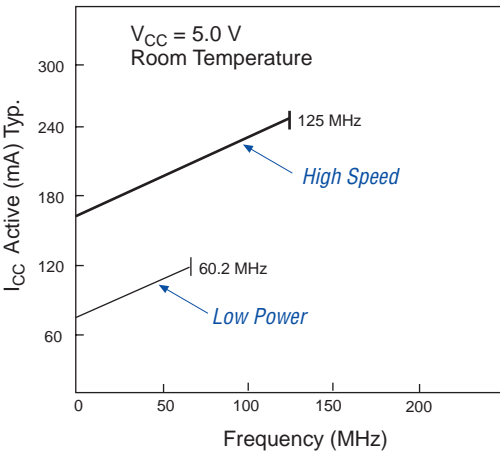
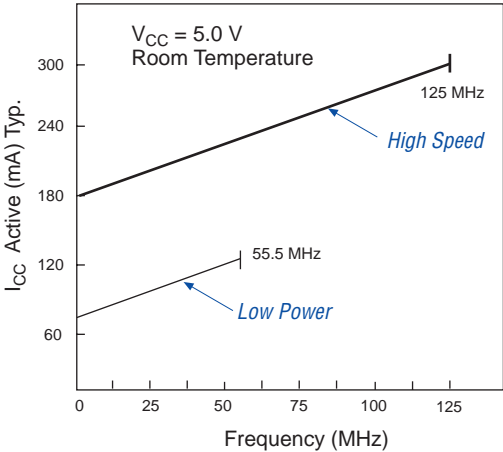


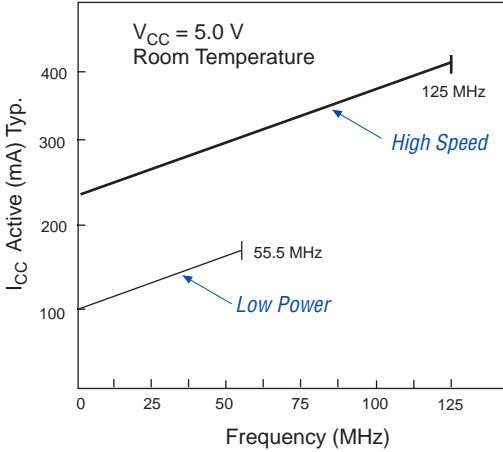
Figure 17. I_{CC} vs. Frequency for MAX 7000S Devices (Part 2 of 2)

Information on MAX 7000S devices is preliminary.

EPM7192S



EPM7256S



Device Pin-Outs

Tables 7 through 21 show the pin names and numbers for the pins in each MAX 7000 device package.

| <i>Table 7. EPM7032, EPM7032V & EPM7032S Dedicated Pin-Outs</i> | | |
|---|----------------|----------------------|
| Pin Name | 44-Pin J-Lead | 44-Pin PQFP/TQFP,(1) |
| INPUT/GCLK1 | 43 | 37 |
| INPUT/GCLKn | 1 | 39 |
| INPUT/OE1 | 44 | 38 |
| INPUT/OE2/GCLK2 (2) | 2 | 40 |
| TDI (3) | 7 | 1 |
| TMS (3) | 13 | 7 |
| TCK (3) | 32 | 26 |
| TDO (3) | 38 | 32 |
| PDn (4) | 3 | 41 |
| GND | 10, 22, 30, 42 | 4, 16, 24, 36 |
| VCC (4) | 3, 15, 23, 35 | 9, 17, 29, 41 |
| No Connect (N.C.) | — | — |
| Total User I/O Pins | 32 | 32 |

Table 8. EPM7032, EPM7032V & EPM7032S I/O Pin-Outs *Note (2)*

| MC | LAB | 44-Pin J-Lead | 44-Pin PQFP/TQFP, (1) | MC | LAB | 44-Pin J-Lead | 44-Pin PQFP/TQFP, (1) |
|----|-----|------------------|--------------------------|----|-----|------------------|--------------------------|
| 1 | A | 4 | 42 | 17 | B | 41 | 35 |
| 2 | A | 5 | 43 | 18 | B | 40 | 34 |
| 3 | A | 6 | 44 | 19 | B | 39 | 33 |
| 4 | A | 7 (3) | 1 (3) | 20 | B | 38 (3) | 32 (3) |
| 5 | A | 8 | 2 | 21 | B | 37 | 31 |
| 6 | A | 9 | 3 | 22 | B | 36 | 30 |
| 7 | A | 11 | 5 | 23 | B | 34 | 28 |
| 8 | A | 12 | 6 | 24 | B | 33 | 27 |
| 9 | A | 13 (3) | 7 (3) | 25 | B | 32 (3) | 26 (3) |
| 10 | A | 14 | 8 | 26 | B | 31 | 25 |
| 11 | A | 16 | 10 | 27 | B | 29 | 23 |
| 12 | A | 17 | 11 | 28 | B | 28 | 22 |
| 13 | A | 18 | 12 | 29 | B | 27 | 21 |
| 14 | A | 19 | 13 | 30 | B | 26 | 20 |
| 15 | A | 20 | 14 | 31 | B | 25 | 19 |
| 16 | A | 21 | 15 | 32 | B | 24 | 18 |

Notes to tables:

- (1) The 44-pin PQFP package is not offered for EPM7032S devices.
- (2) The GCLK2 function is available in MAX 7000S devices only.
- (3) This JTAG pin applies to only MAX 7000S devices. In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.
- (4) This PDn is available in EPM7032V devices.

Table 9. EPM7064 & EPM7064S Dedicated Pin-Outs *Note (1)*

| Dedicated Pin | 44-Pin J-Lead | 44-Pin TQFP | 68-Pin J-Lead, (2) | 84-Pin J-Lead | 100-Pin TQFP | 100-Pin PQFP, (2) |
|------------------------|-------------------|------------------|-------------------------------------|-------------------------------------|--|--|
| INPUT/GCLK1 | 43 | 37 | 67 | 83 | 87 | 89 |
| INPUT/GCLRn | 1 | 39 | 1 | 1 | 89 | 91 |
| INPUT/OE1 | 44 | 38 | 68 | 84 | 88 | 90 |
| INPUT/OE2/GCLK2 (1) | 2 | 40 | 2 | 2 | 90 | 92 |
| TDI (3) | 7 | 1 | 12 | 14 | 4 | 6 |
| TMS (3) | 13 | 7 | 19 | 23 | 15 | 17 |
| TCK (3) | 32 | 26 | 50 | 62 | 62 | 64 |
| TDO (3) | 38 | 32 | 57 | 71 | 73 | 75 |
| GND | 10, 22, 30, 42 | 4, 16, 24, 36 | 6, 16, 26, 34, 38, 48, 58, 66 | 7, 19, 32, 42, 47, 59, 72, 82 | 38, 86, 11, 26, 43, 59, 74, 95 | 13, 28, 40, 45, 61, 76, 88, 97 |
| VCCINT (5.0 V only) | 3, 15, 23, 35 | 9, 17, 29, 41 | 3, 35 | 3, 43 | 39, 91 | 41, 93 |
| VCCIO (3.3 V or 5.0 V) | — | — | 11, 21, 31, 43, 53, 63 | 13, 26, 38, 53, 66, 78 | 3, 18, 34, 51, 66, 82 | 5, 20, 36, 53, 68, 84 |
| No Connect (N.C.) | — | — | — | — | 1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78 | 1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80 |
| Total User I/O Pins | 32 | 32 | 48 | 64 | 64 | 64 |

Table 10. EPM7064 & EPM7064S I/O Pin-Outs (44-Pin J-Lead, 44-Pin TQFP & 68-Pin J-Lead Packages)

| MC | LAB | 44-Pin J-Lead | 44-Pin TQFP | 68-Pin J-Lead, (2) | MC | LAB | 44-Pin J-Lead | 44-Pin TQFP | 68-Pin J-Lead, (2) |
|----|-----|------------------|----------------|-----------------------|----|-----|------------------|----------------|-----------------------|
| 1 | A | 12 | 6 | 18 | 17 | B | 21 | 15 | 33 |
| 2 | A | — | — | — | 18 | B | — | — | — |
| 3 | A | 11 | 5 | 17 | 19 | B | 20 | 14 | 32 |
| 4 | A | 9 | 3 | 15 | 20 | B | 19 | 13 | 30 |
| 5 | A | 8 | 2 | 14 | 21 | B | 18 | 12 | 29 |
| 6 | A | — | — | 13 | 22 | B | — | — | 28 |
| 7 | A | — | — | — | 23 | B | — | — | — |
| 8 | A | 7 (3) | 1 (3) | 12 (3) | 24 | B | 17 | 11 | 27 |
| 9 | A | — | — | 10 | 25 | B | 16 | 10 | 25 |
| 10 | A | — | — | — | 26 | B | — | — | — |
| 11 | A | 6 | 44 | 9 | 27 | B | — | — | 24 |
| 12 | A | — | — | 8 | 28 | B | — | — | 23 |
| 13 | A | — | — | 7 | 29 | B | — | — | 22 |
| 14 | A | 5 | 43 | 5 | 30 | B | 14 | 8 | 20 |
| 15 | A | — | — | — | 31 | B | — | — | — |
| 16 | A | 4 | 42 | 4 | 32 | B | 13 (3) | 7 (3) | 19 (3) |
| 33 | C | 24 | 18 | 36 | 49 | D | 33 | 27 | 51 |
| 34 | C | — | — | — | 50 | D | — | — | — |
| 35 | C | 25 | 19 | 37 | 51 | D | 34 | 28 | 52 |
| 36 | C | 26 | 20 | 39 | 52 | D | 36 | 30 | 54 |
| 37 | C | 27 | 21 | 40 | 53 | D | 37 | 31 | 55 |
| 38 | C | — | — | 41 | 54 | D | — | — | 56 |
| 39 | C | — | — | — | 55 | D | — | — | — |
| 40 | C | 28 | 22 | 42 | 56 | D | 38 (3) | 32 (3) | 57 (3) |
| 41 | C | 29 | 23 | 44 | 57 | D | 39 | 33 | 59 |
| 42 | C | — | — | — | 58 | D | — | — | — |
| 43 | C | — | — | 45 | 59 | D | — | — | 60 |
| 44 | C | — | — | 46 | 60 | D | — | — | 61 |
| 45 | C | — | — | 47 | 61 | D | — | — | 62 |
| 46 | C | 31 | 25 | 49 | 62 | D | 40 | 34 | 64 |
| 47 | C | — | — | — | 63 | D | — | — | — |
| 48 | C | 32 (3) | 26 (3) | 50 (3) | 64 | D | 41 | 35 | 65 |

Table 11. EPM7064 & EPM7064S I/O Pin-Outs (84-Pin J-Lead, 100-Pin TQFP & 100-Pin PQFP Packages)

| MC | LAB | 84-Pin J-Lead | 100-Pin TQFP | 100-Pin PQFP, (2) | MC | LAB | 84-Pin J-Lead | 100-Pin TQFP | 100-Pin PQFP, (2) |
|----|-----|------------------|-----------------|----------------------|----|-----|------------------|-----------------|----------------------|
| 1 | A | 22 | 14 | 16 | 17 | B | 41 | 37 | 39 |
| 2 | A | 21 | 13 | 15 | 18 | B | 40 | 36 | 38 |
| 3 | A | 20 | 12 | 14 | 19 | B | 39 | 35 | 37 |
| 4 | A | 18 | 10 | 12 | 20 | B | 37 | 33 | 35 |
| 5 | A | 17 | 9 | 11 | 21 | B | 36 | 32 | 34 |
| 6 | A | 16 | 8 | 10 | 22 | B | 35 | 31 | 33 |
| 7 | A | 15 | 6 | 8 | 23 | B | 34 | 30 | 32 |
| 8 | A | 14 (3) | 4 (3) | 6 (3) | 24 | B | 33 | 29 | 31 |
| 9 | A | 12 | 100 | 4 | 25 | B | 31 | 25 | 27 |
| 10 | A | 11 | 99 | 3 | 26 | B | 30 | 23 | 25 |
| 11 | A | 10 | 98 | 100 | 27 | B | 29 | 21 | 23 |
| 12 | A | 9 | 97 | 99 | 28 | B | 28 | 20 | 22 |
| 13 | A | 8 | 96 | 98 | 29 | B | 27 | 19 | 21 |
| 14 | A | 6 | 94 | 96 | 30 | B | 25 | 17 | 19 |
| 15 | A | 5 | 93 | 95 | 31 | B | 24 | 16 | 18 |
| 16 | A | 4 | 92 | 94 | 32 | B | 23 (3) | 15 (3) | 17 (3) |
| 33 | C | 44 | 40 | 42 | 49 | D | 63 | 63 | 65 |
| 34 | C | 45 | 41 | 43 | 50 | D | 64 | 64 | 66 |
| 35 | C | 46 | 42 | 44 | 51 | D | 65 | 65 | 67 |
| 36 | C | 48 | 44 | 46 | 52 | D | 67 | 67 | 69 |
| 37 | C | 49 | 45 | 47 | 53 | D | 68 | 68 | 70 |
| 38 | C | 50 | 46 | 48 | 54 | D | 69 | 69 | 71 |
| 39 | C | 51 | 47 | 49 | 55 | D | 70 | 71 | 73 |
| 40 | C | 52 | 48 | 50 | 56 | D | 71 (3) | 73 (3) | 75 (3) |
| 41 | C | 54 | 52 | 54 | 57 | D | 73 | 75 | 77 |
| 42 | C | 55 | 54 | 56 | 58 | D | 74 | 76 | 78 |
| 43 | C | 56 | 56 | 58 | 59 | D | 75 | 79 | 81 |
| 44 | C | 57 | 57 | 59 | 60 | D | 76 | 80 | 82 |
| 45 | C | 58 | 58 | 60 | 61 | D | 77 | 81 | 83 |
| 46 | C | 60 | 60 | 62 | 62 | D | 79 | 83 | 85 |
| 47 | C | 61 | 61 | 63 | 63 | D | 80 | 84 | 86 |
| 48 | C | 62 (3) | 62 (3) | 64 (3) | 64 | D | 81 | 85 | 87 |

Notes to tables:

- (1) The GCLK2 function is available in MAX 7000S devices only.
- (2) This package is not offered for EPM7064S devices.
- (3) This JTAG pin applies to only MAX 7000S devices. In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 12. EPM7096 Dedicated Pin-Outs

| Dedicated Pin | 68-Pin J-Lead | 84-Pin J-Lead | 100-Pin PQFP |
|-------------------------|----------------------------------|----------------------------------|-----------------------------------|
| INPUT/GCLK1 | 67 | 83 | 89 |
| INPUT/GCLK _n | 1 | 1 | 91 |
| INPUT/OE1 | 68 | 84 | 90 |
| INPUT/OE2/GCLK2 | 2 | 2 | 92 |
| GND | 6, 16, 26, 34, 38, 48, 58, 66 | 7, 19, 32, 42, 47, 59, 72, 82 | 13, 28, 40, 45, 61, 76, 88, 97 |
| VCCINT (5.0 V only) | 3, 35 | 3, 43 | 41, 93 |
| VCCIO (3.3 V or 5.0 V) | 11, 21, 31, 43, 53, 63 | 13, 26, 38, 53, 66, 78 | 5, 20, 36, 53, 68, 84 |
| No Connect (N.C.) | – | 6, 39, 46, 79 | 9, 24, 37, 44, 57, 72, 85, 96 |
| Total User I/O Pins | 48 | 60 | 72 |

Table 13. EPM7096 I/O Pin-Outs (Part 1 of 2)

| MC | LAB | 68-Pin J-Lead | 84-Pin J-Lead | 100-Pin PQFP | MC | LAB | 68-Pin J-Lead | 84-Pin J-Lead | 100-Pin PQFP |
|----|-----|------------------|------------------|-----------------|----|-----|------------------|------------------|-----------------|
| 1 | A | 13 | 16 | 8 | 17 | B | 23 | 28 | 23 |
| 2 | A | – | – | – | 18 | B | – | – | – |
| 3 | A | – | 15 | 7 | 19 | B | 22 | 27 | 22 |
| 4 | A | 12 | 14 | 6 | 20 | B | – | – | 21 |
| 5 | A | – | – | 4 | 21 | B | 20 | 25 | 19 |
| 6 | A | 10 | 12 | 3 | 22 | B | – | 24 | 18 |
| 7 | A | – | – | – | 23 | B | – | – | – |
| 8 | A | 9 | 11 | 2 | 24 | B | 19 | 23 | 17 |
| 9 | A | 8 | 10 | 1 | 25 | B | 18 | 22 | 16 |
| 10 | A | – | – | – | 26 | B | – | – | – |
| 11 | A | – | 9 | 100 | 27 | B | 17 | 21 | 15 |
| 12 | A | 7 | 8 | 99 | 28 | B | – | 20 | 14 |
| 13 | A | – | – | 98 | 29 | B | 15 | 18 | 12 |
| 14 | A | 5 | 5 | 95 | 30 | B | – | – | 11 |
| 15 | A | – | – | – | 31 | B | – | – | – |
| 16 | A | 4 | 4 | 94 | 32 | B | 14 | 17 | 10 |

Table 13. EPM7096 I/O Pin-Outs (Part 2 of 2)

| MC | LAB | 68-Pin J-Lead | 84-Pin J-Lead | 100-Pin PQFP | MC | LAB | 68-Pin J-Lead | 84-Pin J-Lead | 100-Pin PQFP |
|----|-----|------------------|------------------|-----------------|----|-----|------------------|------------------|-----------------|
| 33 | C | 33 | 41 | 39 | 49 | D | 36 | 44 | 42 |
| 34 | C | — | — | — | 50 | D | — | — | — |
| 35 | C | 32 | 40 | 38 | 51 | D | 37 | 45 | 43 |
| 36 | C | — | — | 35 | 52 | D | — | — | 46 |
| 37 | C | 30 | 37 | 34 | 53 | D | 39 | 48 | 47 |
| 38 | C | — | 36 | 33 | 54 | D | — | 49 | 48 |
| 39 | C | — | — | — | 55 | D | — | — | — |
| 40 | C | 29 | 35 | 32 | 56 | D | 40 | 50 | 49 |
| 41 | C | 28 | 34 | 31 | 57 | D | 41 | 51 | 50 |
| 42 | C | — | — | — | 58 | D | — | — | — |
| 43 | C | 27 | 33 | 30 | 59 | D | 42 | 52 | 51 |
| 44 | C | — | — | 29 | 60 | D | — | — | 52 |
| 45 | C | 25 | 31 | 27 | 61 | D | 44 | 54 | 54 |
| 46 | C | — | 30 | 26 | 62 | D | — | 55 | 55 |
| 47 | C | — | — | — | 63 | D | — | — | — |
| 48 | C | 24 | 29 | 25 | 64 | D | 45 | 56 | 56 |
| 65 | E | 46 | 57 | 58 | 81 | F | 56 | 69 | 73 |
| 66 | E | — | — | — | 82 | F | — | — | — |
| 67 | E | 47 | 58 | 59 | 83 | F | — | 70 | 74 |
| 68 | E | — | — | 60 | 84 | F | 57 | 71 | 75 |
| 69 | E | 49 | 60 | 62 | 85 | F | — | — | 77 |
| 70 | E | — | 61 | 63 | 86 | F | 59 | 73 | 78 |
| 71 | E | — | — | — | 87 | F | — | — | — |
| 72 | E | 50 | 62 | 64 | 88 | F | 60 | 74 | 79 |
| 73 | E | 51 | 63 | 65 | 89 | F | 61 | 75 | 80 |
| 74 | E | — | — | — | 90 | F | — | — | — |
| 75 | E | 52 | 64 | 66 | 91 | F | — | 76 | 81 |
| 76 | E | — | 65 | 67 | 92 | F | 62 | 77 | 82 |
| 77 | E | 54 | 67 | 69 | 93 | F | — | — | 83 |
| 78 | E | — | — | 70 | 94 | F | 64 | 80 | 86 |
| 79 | E | — | — | — | 95 | F | — | — | — |
| 80 | E | 55 | 68 | 71 | 96 | F | 65 | 81 | 87 |

Table 14. EPM7128E & EPM7128S Dedicated Pin-Outs

| Dedicated Pin | 84-Pin J-Lead | 100-Pin PQFP | 100-Pin TQFP, (1) | 160-Pin PQFP |
|------------------------|------------------------|------------------------|------------------------|--|
| INPUT/GCLK1 | 83 | 89 | 87 | 139 |
| INPUT/GCLRn | 1 | 91 | 89 | 141 |
| INPUT/OE1 | 84 | 90 | 88 | 140 |
| INPUT/OE2/GCLK2 | 2 | 92 | 90 | 142 |
| TDI <i>Note (2)</i> | 14 | 6 | 4 | 9 |
| TMS <i>Note (2)</i> | 23 | 17 | 15 | 22 |
| TCK <i>Note (2)</i> | 62 | 64 | 62 | 99 |
| TDO <i>Note (2)</i> | 71 | 75 | 73 | 112 |
| GNDINT | 42, 82 | 40, 88 | 38, 86 | 60, 138 |
| GNDIO | 7, 19, 32, 47, 59, 72 | 13, 28, 45, 61, 76, 97 | 11, 26, 43, 59, 74, 95 | 17, 42, 66, 95, 113, 148 |
| VCCINT (5.0 V only) | 3, 43 | 41, 93 | 39, 91 | 61, 143 |
| VCCIO (3.3 V or 5.0 V) | 13, 26, 38, 53, 66, 78 | 5, 20, 36, 53, 68, 84 | 3, 18, 34, 51, 66, 82 | 8, 26, 55, 79, 104, 133 |
| No Connect (N.C.) | — | — | — | 1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157 |
| Total User I/O Pins | 64 | 80 | 80 | 96 |

Table 15. EPM7128E & EPM7128S I/O Pin-Outs (Part 1 of 2) *Note (2)*

| MC | LAB | 84-Pin J-Lead | 100-Pin PQFP | 100-Pin TQFP, (1) | 160-Pin PQFP | MC | LAB | 84-Pin J-Lead | 100-Pin PQFP | 100-Pin TQFP, (1) | 160-Pin PQFP |
|----|-----|------------------|-----------------|----------------------|-----------------|----|-----|------------------|-----------------|----------------------|-----------------|
| 1 | A | — | 4 | 2 | 160 | 17 | B | 22 | 16 | 14 | 21 |
| 2 | A | — | — | — | — | 18 | B | — | — | — | — |
| 3 | A | 12 | 3 | 1 | 159 | 19 | B | 21 | 15 | 13 | 20 |
| 4 | A | — | — | — | 158 | 20 | B | — | — | — | 19 |
| 5 | A | 11 | 2 | 100 | 153 | 21 | B | 20 | 14 | 12 | 18 |
| 6 | A | 10 | 1 | 99 | 152 | 22 | B | — | 12 | 10 | 16 |
| 7 | A | — | — | — | — | 23 | B | — | — | — | — |
| 8 | A | 9 | 100 | 98 | 151 | 24 | B | 18 | 11 | 9 | 15 |
| 9 | A | — | 99 | 97 | 150 | 25 | B | 17 | 10 | 8 | 14 |
| 10 | A | — | — | — | — | 26 | B | — | — | — | — |
| 11 | A | 8 | 98 | 96 | 149 | 27 | B | 16 | 9 | 7 | 13 |
| 12 | A | — | — | — | 147 | 28 | B | — | — | — | 12 |
| 13 | A | 6 | 96 | 94 | 146 | 29 | B | 15 | 8 | 6 | 11 |
| 14 | A | 5 | 95 | 93 | 145 | 30 | B | — | 7 | 5 | 10 |
| 15 | A | — | — | — | — | 31 | B | — | — | — | — |
| 16 | A | 4 | 94 | 92 | 144 | 32 | B | 14 (3) | 6 (3) | 4 (3) | 9 (3) |
| 33 | C | — | 27 | 25 | 41 | 49 | D | 41 | 39 | 37 | 59 |
| 34 | C | — | — | — | — | 50 | D | — | — | — | — |
| 35 | C | 31 | 26 | 24 | 33 | 51 | D | 40 | 38 | 36 | 58 |
| 36 | C | — | — | — | 32 | 52 | D | — | — | — | 57 |
| 37 | C | 30 | 25 | 23 | 31 | 53 | D | 39 | 37 | 35 | 56 |
| 38 | C | 29 | 24 | 22 | 30 | 54 | D | — | 35 | 33 | 54 |
| 39 | C | — | — | — | — | 55 | D | — | — | — | — |
| 40 | C | 28 | 23 | 21 | 29 | 56 | D | 37 | 34 | 32 | 53 |
| 41 | C | — | 22 | 20 | 28 | 57 | D | 36 | 33 | 31 | 52 |
| 42 | C | — | — | — | — | 58 | D | — | — | — | — |
| 43 | C | 27 | 21 | 19 | 27 | 59 | D | 35 | 32 | 30 | 51 |
| 44 | C | — | — | — | 25 | 60 | D | — | — | — | 50 |
| 45 | C | 25 | 19 | 17 | 24 | 61 | D | 34 | 31 | 29 | 49 |
| 46 | C | 24 | 18 | 16 | 23 | 62 | D | — | 30 | 28 | 48 |
| 47 | C | — | — | — | — | 63 | D | — | — | — | — |
| 48 | C | 23 (3) | 17 (3) | 15 (3) | 22 (3) | 64 | D | 33 | 29 | 27 | 43 |

Table 15. EPM7128E & EPM7128S I/O Pin-Outs (Part 2 of 2) *Note (2)*

| MC | LAB | 84-Pin J-Lead | 100-Pin PQFP | 100-Pin TQFP, (1) | 160-Pin PQFP | MC | LAB | 84-Pin J-Lead | 100-Pin PQFP | 100-Pin TQFP, (1) | 160-Pin PQFP |
|-----|-----|------------------|-----------------|----------------------|-----------------|-----|-----|------------------|-----------------|----------------------|-----------------|
| 65 | E | 44 | 42 | 40 | 62 | 81 | F | — | 54 | 52 | 80 |
| 66 | E | — | — | — | — | 82 | F | — | — | — | — |
| 67 | E | 45 | 43 | 41 | 63 | 83 | F | 54 | 55 | 53 | 88 |
| 68 | E | — | — | — | 64 | 84 | F | — | — | — | 89 |
| 69 | E | 46 | 44 | 42 | 65 | 85 | F | 55 | 56 | 54 | 90 |
| 70 | E | — | 46 | 44 | 67 | 86 | F | 56 | 57 | 55 | 91 |
| 71 | E | — | — | — | — | 87 | F | — | — | — | — |
| 72 | E | 48 | 47 | 45 | 68 | 88 | F | 57 | 58 | 56 | 92 |
| 73 | E | 49 | 48 | 46 | 69 | 89 | F | — | 59 | 57 | 93 |
| 74 | E | — | — | — | — | 90 | F | — | — | — | — |
| 75 | E | 50 | 49 | 47 | 70 | 91 | F | 58 | 60 | 58 | 94 |
| 76 | E | — | — | — | 71 | 92 | F | — | — | — | 96 |
| 77 | E | 51 | 50 | 48 | 72 | 93 | F | 60 | 62 | 60 | 97 |
| 78 | E | — | 51 | 49 | 73 | 94 | F | 61 | 63 | 61 | 98 |
| 79 | E | — | — | — | — | 95 | F | — | — | — | — |
| 80 | E | 52 | 52 | 50 | 78 | 96 | F | 62 (3) | 64 (3) | 62 (3) | 99 (3) |
| 97 | G | 63 | 65 | 63 | 100 | 113 | H | — | 77 | 75 | 121 |
| 98 | G | — | — | — | — | 114 | H | — | — | — | — |
| 99 | G | 64 | 66 | 64 | 101 | 115 | H | 73 | 78 | 76 | 122 |
| 100 | G | — | — | — | 102 | 116 | H | — | — | — | 123 |
| 101 | G | 65 | 67 | 65 | 103 | 117 | H | 74 | 79 | 77 | 128 |
| 102 | G | — | 69 | 67 | 105 | 118 | H | 75 | 80 | 78 | 129 |
| 103 | G | — | — | — | — | 119 | H | — | — | — | — |
| 104 | G | 67 | 70 | 68 | 106 | 120 | H | 76 | 81 | 79 | 130 |
| 105 | G | 68 | 71 | 69 | 107 | 121 | H | — | 82 | 80 | 131 |
| 106 | G | — | — | — | — | 122 | H | — | — | — | — |
| 107 | G | 69 | 72 | 70 | 108 | 123 | H | 77 | 83 | 81 | 132 |
| 108 | G | — | — | — | 109 | 124 | H | — | — | — | 134 |
| 109 | G | 70 | 73 | 71 | 110 | 125 | H | 79 | 85 | 83 | 135 |
| 110 | G | — | 74 | 72 | 111 | 126 | H | 80 | 86 | 84 | 136 |
| 111 | G | — | — | — | — | 127 | H | — | — | — | — |
| 112 | G | 71 (3) | 75 (3) | 73 (3) | 112 (3) | 128 | H | 81 | 87 | 85 | 137 |

Notes to tables:

- (1) A complete thermal analysis should be performed before committing a design to this device package.
- (2) Information on MAX 7000S devices is preliminary.
- (3) This JTAG pin applies to only MAX 7000S devices. In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for boundary-scan testing or for ISP, this pin is not available as a user I/O pin.

Table 16. EPM7160E & EPM7160S Dedicated Pin-Outs *Note (1)*

| Dedicated Pin | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP |
|------------------------|----------------------------------|-----------------------------------|-----------------------------------|---|
| INPUT/GCLK1 | 83 | 87 | 89 | 139 |
| INPUT/GCLRn | 1 | 89 | 91 | 141 |
| INPUT/OE1 | 84 | 88 | 90 | 140 |
| INPUT/OE2/GCLK2 | 2 | 90 | 92 | 142 |
| TDI (1) | 14 | 4 | 6 | 9 |
| TMS (1) | 23 | 15 | 17 | 22 |
| TCK (1) | 62 | 62 | 64 | 99 |
| TDO (1) | 71 | 73 | 75 | 112 |
| GND | 7, 19, 32, 42, 47, 59, 72, 82 | 38, 86, 11, 26, 43, 59, 74, 95 | 13, 28, 40, 45, 61, 76, 88, 97 | 17, 42, 60, 66, 95, 113, 138, 148 |
| VCCINT (5.0 V only) | 3, 43 | 39,91 | 41, 93 | 61, 143 |
| VCCIO (3.3 V or 5.0 V) | 13, 26, 38, 53, 66, 78 | 3, 18, 34, 51, 66, 82 | 5, 20, 36, 53, 68, 84 | 8, 26, 55, 79, 104, 133 |
| No Connect (N.C.) | 6, 39, 46, 79 | — | — | 1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157 |
| Total User I/O Pins | 60 | 80 | 80 | 100 |

Table 17. EPM7160E & EPM7160S I/O Pin-Outs (Part 1 of 3)

| MC | LAB | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP | MC | LAB | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP |
|----|-----|------------------|----------------------|----------------------|-----------------|----|-----|------------------|----------------------|----------------------|-----------------|
| 1 | A | 11 | 100 | 2 | 158 | 17 | B | 18 | 9 | 11 | 15 |
| 2 | A | — | — | — | — | 18 | B | — | — | — | — |
| 3 | A | 10 | 99 | 1 | 153 | 19 | B | 17 | 8 | 10 | 14 |
| 4 | A | — | — | — | — | 20 | B | — | — | — | — |
| 5 | A | — | — | — | 152 | 21 | B | — | — | — | 13 |
| 6 | A | — | 98 | 100 | 151 | 22 | B | — | 7 | 9 | 12 |
| 7 | A | — | — | — | — | 23 | B | — | — | — | — |
| 8 | A | 9 | 97 | 99 | 150 | 24 | B | 16 | 6 | 8 | 11 |
| 9 | A | 8 | 96 | 98 | 149 | 25 | B | 15 | 5 | 7 | 10 |
| 10 | A | — | — | — | — | 26 | B | — | — | — | — |
| 11 | A | 5 | 94 | 96 | 147 | 27 | B | 14 (1) | 4 (1) | 6 (1) | 9 (1) |
| 12 | A | — | — | — | — | 28 | B | — | — | — | — |

Table 17. EPM7160E & EPM7160S I/O Pin-Outs (Part 2 of 3)

| MC | LAB | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP | MC | LAB | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP |
|----|-----|------------------|----------------------|----------------------|-----------------|----|-----|------------------|----------------------|----------------------|-----------------|
| 13 | A | — | — | — | 146 | 29 | B | — | — | — | 7 |
| 14 | A | — | 93 | 95 | 145 | 30 | B | — | 2 | 4 | 160 |
| 15 | A | — | — | — | — | 31 | B | — | — | — | — |
| 16 | A | 4 | 92 | 94 | 144 | 32 | B | 12 | 1 | 3 | 159 |
| 33 | C | — | 19 | 21 | 27 | 49 | D | — | — | — | 48 |
| 34 | C | — | — | — | — | 50 | D | — | — | — | — |
| 35 | C | 25 | 17 | 19 | 25 | 51 | D | 33 | 28 | 30 | 44 |
| 36 | C | — | — | — | — | 52 | D | — | — | — | — |
| 37 | C | — | — | — | 24 | 53 | D | — | 27 | 29 | 43 |
| 38 | C | 24 | 16 | 18 | 23 | 54 | D | 31 | 25 | 27 | 41 |
| 39 | C | — | — | — | — | 55 | D | — | — | — | — |
| 40 | C | 23 (1) | 15 (1) | 17 (1) | 22 (1) | 56 | D | 30 | 24 | 26 | 33 |
| 41 | C | — | 10 | 12 | 16 | 57 | D | — | — | — | 32 |
| 42 | C | — | — | — | — | 58 | D | — | — | — | — |
| 43 | C | 20 | 12 | 14 | 18 | 59 | D | 29 | 23 | 25 | 31 |
| 44 | C | — | — | — | — | 60 | D | — | — | — | — |
| 45 | C | — | — | — | 19 | 61 | D | — | 22 | 24 | 30 |
| 46 | C | 21 | 13 | 15 | 20 | 62 | D | 28 | 21 | 23 | 29 |
| 47 | C | — | — | — | — | 63 | D | — | — | — | — |
| 48 | C | 22 | 14 | 16 | 21 | 64 | D | 27 | 20 | 22 | 28 |
| 65 | E | — | — | — | 59 | 81 | F | — | — | — | 62 |
| 66 | E | — | — | — | — | 82 | F | — | — | — | — |
| 67 | E | 41 | 37 | 39 | 58 | 83 | F | 44 | 40 | 42 | 63 |
| 68 | E | — | — | — | — | 84 | F | — | — | — | — |
| 69 | E | — | 36 | 38 | 57 | 85 | F | — | 41 | 43 | 64 |
| 70 | E | 40 | 35 | 37 | 56 | 86 | F | 45 | 42 | 44 | 65 |
| 71 | E | — | — | — | — | 87 | F | — | — | — | — |
| 72 | E | 37 | 33 | 35 | 54 | 88 | F | 48 | 44 | 46 | 67 |
| 73 | E | — | — | — | 53 | 89 | F | — | — | — | 68 |
| 74 | E | — | — | — | — | 90 | F | — | — | — | — |
| 75 | E | 36 | 32 | 34 | 52 | 91 | F | 49 | 45 | 47 | 69 |
| 76 | E | — | — | — | — | 92 | F | — | — | — | — |
| 77 | E | — | 31 | 33 | 51 | 93 | F | — | 46 | 48 | 70 |
| 78 | E | 35 | 30 | 32 | 50 | 94 | F | 50 | 47 | 49 | 71 |
| 79 | E | — | — | — | — | 95 | F | — | — | — | — |
| 80 | E | 34 | 29 | 31 | 49 | 96 | F | 51 | 48 | 50 | 72 |

Table 17. EPM7160E & EPM7160S I/O Pin-Outs (Part 3 of 3)

| MC | LAB | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP | MC | LAB | 84-Pin J-Lead | 100-Pin TQFP, (2) | 100-Pin PQFP, (3) | 160-Pin PQFP |
|-----|-----|------------------|----------------------|----------------------|-----------------|-----|-----|------------------|----------------------|----------------------|-----------------|
| 97 | G | — | — | — | 73 | 113 | H | — | 58 | 60 | 94 |
| 98 | G | — | — | — | — | 114 | H | — | — | — | — |
| 99 | G | 52 | 49 | 51 | 77 | 115 | H | 60 | 60 | 62 | 96 |
| 100 | G | — | — | — | — | 116 | H | — | — | — | — |
| 101 | G | — | 50 | 52 | 78 | 117 | H | — | — | — | 97 |
| 102 | G | 54 | 52 | 54 | 80 | 118 | H | 61 | 61 | 63 | 98 |
| 103 | G | — | — | — | — | 119 | H | — | — | — | — |
| 104 | G | 55 | 53 | 55 | 88 | 120 | H | 62 (1) | 62 (1) | 64 (1) | 99 (1) |
| 105 | G | — | — | — | 89 | 121 | H | — | 67 | 69 | 105 |
| 106 | G | — | — | — | — | 122 | H | — | — | — | — |
| 107 | G | 56 | 54 | 56 | 90 | 123 | H | 65 | 65 | 67 | 103 |
| 108 | G | — | — | — | — | 124 | H | — | — | — | — |
| 109 | G | — | 55 | 57 | 91 | 125 | H | — | — | — | 102 |
| 110 | G | 57 | 56 | 58 | 92 | 126 | H | 64 | 64 | 66 | 101 |
| 111 | G | — | — | — | — | 127 | H | — | — | — | — |
| 112 | G | 58 | 57 | 59 | 93 | 128 | H | 63 | 63 | 65 | 100 |
| 129 | I | 67 | 68 | 70 | 106 | 145 | J | 74 | 77 | 79 | 123 |
| 130 | I | — | — | — | — | 146 | J | — | — | — | — |
| 131 | I | 68 | 69 | 71 | 107 | 147 | J | 75 | 78 | 80 | 128 |
| 132 | I | — | — | — | — | 148 | J | — | — | — | — |
| 133 | I | — | — | — | 108 | 149 | J | — | — | — | 129 |
| 134 | I | — | 70 | 72 | 109 | 150 | J | — | 79 | 81 | 130 |
| 135 | I | — | — | — | — | 151 | J | — | — | — | — |
| 136 | I | 69 | 71 | 73 | 110 | 152 | J | 76 | 80 | 82 | 131 |
| 137 | I | 70 | 72 | 74 | 111 | 153 | J | 77 | 81 | 83 | 132 |
| 138 | I | — | — | — | — | 154 | J | — | — | — | — |
| 139 | I | 71 (1) | 73 (1) | 75 (1) | 112 (1) | 155 | J | 80 | 83 | 85 | 134 |
| 140 | I | — | — | — | — | 156 | J | — | — | — | — |
| 141 | I | — | — | — | 114 | 157 | J | — | — | — | 135 |
| 142 | I | — | 75 | 77 | 121 | 158 | J | — | 84 | 86 | 136 |
| 143 | I | — | — | — | — | 159 | J | — | — | — | — |
| 144 | I | 73 | 76 | 78 | 122 | 160 | J | 81 | 85 | 87 | 137 |

Note to tables:

- (1) This JTAG pin applies to only MAX 7000S devices. For MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or with ISP, this pin is not available as a user I/O pin.
- (2) A complete thermal analysis should be performed before committing a design to this device package.
- (3) The 100-pin PQFP is not available for EPM7160S devices.

Table 18. EPM7192E & EPM7192S Dedicated Pin-Outs

| Dedicated Pin | 160-Pin PGA, <i>Note (1)</i> | 160-Pin PQFP |
|------------------------|---|--|
| INPUT/GCLK1 | M8 | 139 |
| INPUT/GCLRn | N8 | 141 |
| INPUT/OE1 | P8 | 140 |
| INPUT/OE2/GCLK2 | R8 | 142 |
| TDI (2) | P9 | 146 |
| TMS (2) | G15 | 23 |
| TCK (2) | G2 | 98 |
| TDO (2) | R7 | 135 |
| GND | C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11 | 3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148 |
| VCCINT (5.0 V only) | C7, C9, N7, N9 | 56, 65, 137, 144 |
| VCCIO (3.3 V or 5.0 V) | C5, C10, C12, D3, G12, H4, J12, M3, N5, N12 | 10, 25, 40, 55, 74, 89, 103, 118, 133, 155 |
| No Connect (N.C.) | A1, A2, A14, A15, R1, R2, R14, R15 | 1, 11, 39, 54, 67, 82, 110, 120 |
| Total User I/O Pins | 120 | 120 |

Table 19. EPM7192E & EPM7192S I/O Pin-Outs (Part 1 of 3)

| MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP | MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP | MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP |
|----|-----|---------------------|-----------------|----|-----|---------------------|-----------------|----|-----|---------------------|-----------------|
| 1 | A | M12 | 156 | 17 | B | L14 | 8 | 33 | C | H14 | 21 |
| 2 | A | — | — | 18 | B | — | — | 34 | C | — | — |
| 3 | A | P11 | 154 | 19 | B | M14 | 7 | 35 | C | J13 | 20 |
| 4 | A | — | — | 20 | B | — | — | 36 | C | — | — |
| 5 | A | P12 | 153 | 21 | B | M15 | 6 | 37 | C | H15 | 19 |
| 6 | A | P10 | 152 | 22 | B | N14 | 5 | 38 | C | J15 | 17 |
| 7 | A | — | — | 23 | B | — | — | 39 | C | — | — |
| 8 | A | R12 | 151 | 24 | B | N15 | 4 | 40 | C | J14 | 16 |
| 9 | A | N10 | 150 | 25 | B | P15 | 2 | 41 | C | K15 | 15 |
| 10 | A | — | — | 26 | B | — | — | 42 | C | — | — |
| 11 | A | R11 | 149 | 27 | B | N13 | 160 | 43 | C | K13 | 14 |
| 12 | A | — | — | 28 | B | — | — | 44 | C | — | — |
| 13 | A | R10 | 147 | 29 | B | P14 | 159 | 45 | C | L15 | 13 |
| 14 | A | P9 (2) | 146 (2) | 30 | B | P13 | 158 | 46 | C | K14 | 12 |
| 15 | A | — | — | 31 | B | — | — | 47 | C | — | — |
| 16 | A | R9 | 145 | 32 | B | R13 | 157 | 48 | C | L13 | 9 |

Table 19. EPM7192E & EPM7192S I/O Pin-Outs (Part 2 of 3)

| MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP | MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP | MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP |
|-----|-----|---------------------|-----------------|-----|-----|---------------------|-----------------|-----|-----|---------------------|-----------------|
| 49 | D | D15 | 33 | 65 | E | B12 | 45 | 81 | F | D8 | 60 |
| 50 | D | — | — | 66 | E | — | — | 82 | F | — | — |
| 51 | D | E15 | 31 | 67 | E | B13 | 44 | 83 | F | A9 | 59 |
| 52 | D | — | — | 68 | E | — | — | 84 | F | — | — |
| 53 | D | E14 | 30 | 69 | E | C13 | 43 | 85 | F | C8 | 58 |
| 54 | D | F15 | 29 | 70 | E | B14 | 42 | 86 | F | B9 | 53 |
| 55 | D | — | — | 71 | E | — | — | 87 | F | — | — |
| 56 | D | F13 | 28 | 72 | E | C14 | 41 | 88 | F | A10 | 52 |
| 57 | D | G14 | 27 | 73 | E | D12 | 38 | 89 | F | B10 | 51 |
| 58 | D | — | — | 74 | E | — | — | 90 | F | — | — |
| 59 | D | F14 | 26 | 75 | E | B15 | 37 | 91 | F | A11 | 50 |
| 60 | D | — | — | 76 | E | — | — | 92 | F | — | — |
| 61 | D | G13 | 24 | 77 | E | D14 | 36 | 93 | F | B11 | 49 |
| 62 | D | G15 (2) | 23 (2) | 78 | E | C15 | 35 | 94 | F | A12 | 48 |
| 63 | D | — | — | 79 | E | — | — | 95 | F | — | — |
| 64 | D | H13 | 22 | 80 | E | E13 | 34 | 96 | F | A13 | 46 |
| 97 | G | A8 | 61 | 113 | H | A3 | 76 | 129 | I | E3 | 88 |
| 98 | G | — | — | 114 | H | — | — | 130 | I | — | — |
| 99 | G | B8 | 62 | 115 | H | B4 | 77 | 131 | I | F3 | 90 |
| 100 | G | — | — | 116 | H | — | — | 132 | I | — | — |
| 101 | G | A7 | 63 | 117 | H | B3 | 78 | 133 | I | E2 | 91 |
| 102 | G | A6 | 68 | 118 | H | C3 | 79 | 134 | I | F2 | 92 |
| 103 | G | — | — | 119 | H | — | — | 135 | I | — | — |
| 104 | G | B7 | 69 | 120 | H | B2 | 80 | 136 | I | E1 | 93 |
| 105 | G | A5 | 70 | 121 | H | B1 | 83 | 137 | I | G3 | 94 |
| 106 | G | — | — | 122 | H | — | — | 138 | I | — | — |
| 107 | G | B6 | 71 | 123 | H | C2 | 84 | 139 | I | F1 | 95 |
| 108 | G | — | — | 124 | H | — | — | 140 | I | — | — |
| 109 | G | A4 | 72 | 125 | H | C1 | 85 | 141 | I | G1 | 97 |
| 110 | G | B5 | 73 | 126 | H | D2 | 86 | 142 | I | G2 (2) | 98 (2) |
| 111 | G | — | — | 127 | H | — | — | 143 | I | — | — |
| 112 | G | D4 | 75 | 128 | H | D1 | 87 | 144 | I | H1 | 99 |

Table 19. EPM7192E & EPM7192S I/O Pin-Outs (Part 3 of 3)

| MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP | MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP | MC | LAB | 160-Pin PGA, (1) | 160-Pin PQFP |
|-----|-----|---------------------|-----------------|-----|-----|---------------------|-----------------|-----|-----|---------------------|-----------------|
| 145 | J | H2 | 100 | 161 | K | L2 | 113 | 177 | L | R3 | 125 |
| 146 | J | — | — | 162 | K | — | — | 178 | L | — | — |
| 147 | J | J1 | 101 | 163 | K | N1 | 114 | 179 | L | R4 | 127 |
| 148 | J | — | — | 164 | K | — | — | 180 | L | — | — |
| 149 | J | H3 | 102 | 165 | K | L3 | 115 | 181 | L | M4 | 128 |
| 150 | J | J3 | 104 | 166 | K | P1 | 116 | 182 | L | R5 | 129 |
| 151 | J | — | — | 167 | K | — | — | 183 | L | — | — |
| 152 | J | K1 | 105 | 168 | K | M2 | 117 | 184 | L | P5 | 130 |
| 153 | J | J2 | 106 | 169 | K | N2 | 119 | 185 | L | R6 | 131 |
| 154 | J | — | — | 170 | K | — | — | 186 | L | — | — |
| 155 | J | K2 | 107 | 171 | K | P2 | 121 | 187 | L | P6 | 132 |
| 156 | J | — | — | 172 | K | — | — | 188 | L | — | — |
| 157 | J | K3 | 108 | 173 | K | N3 | 122 | 189 | L | N6 | 134 |
| 158 | J | L1 | 109 | 174 | K | P3 | 123 | 190 | L | R7 (2) | 135 (2) |
| 159 | J | — | — | 175 | K | — | — | 191 | L | — | — |
| 160 | J | M1 | 112 | 176 | K | P4 | 124 | 192 | L | P7 | 136 |

Notes to tables:

- (1) This package is not offered for EPM7192S devices.
- (2) This JTAG pin applies to only MAX 7000S devices. For MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 20. EPM7256E & EPM7256S Dedicated Pin-Outs

| Dedicated Pin | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP |
|------------------------|--|---|---|
| INPUT/GCLK1 | 139 | P9 | 184 |
| INPUT/GCLRn | 141 | R9 | 182 |
| INPUT/OE1 | 140 | T9 | 183 |
| INPUT/OE2/GCLK2 | 142 | U9 | 181 |
| TDI, Note (3) | 146 | U10 | 176 |
| TMS, Note (3) | 23 | H15 | 127 |
| TCK, Note (3) | 98 | H3 | 30 |
| TDO, Note (3) | 135 | U8 | 189 |
| GND | 3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148 | C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11 | 14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200 |
| VCCINT (5.0 V only) | 56, 65, 137, 144 | D7, D11, P7, P11 | 74, 83, 179, 186 |
| VCCIO (3.3 V or 5.0 V) | 10, 25, 40, 55, 74, 89, 103, 118, 133, 155 | C5, C11, D14, G4, H14, K4, L14, P3, R5, R14 | 5, 23, 41, 63, 85, 107, 125, 143, 165, 191 |
| No Connect (N.C.) | — | — | 1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208. |
| Total User I/O Pins | 128 | 160 | 160 |

Table 21. EPM7256E & EPM7256S I/O Pin-Outs (Part 1 of 5)

| MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP | MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP |
|----|-----|------------------------------|------------------------|----------------------|----|-----|------------------------------|------------------------|----------------------|
| 1 | A | 2 | U17 | 153 | 17 | B | 12 | N17 | 141 |
| 2 | A | — | — | — | 18 | B | — | — | — |
| 3 | A | 1 | R16 | 154 | 19 | B | 11 | M16 | 142 |
| 4 | A | — | — | — | 20 | B | — | — | — |
| 5 | A | 160 | P14 | 159 | 21 | B | 9 | M15 | 144 |
| 6 | A | — | U16 | 160 | 22 | B | — | P17 | 145 |
| 7 | A | — | — | — | 23 | B | — | — | — |
| 8 | A | 159 | R15 | 161 | 24 | B | 8 | N16 | 146 |
| 9 | A | 158 | U15 | 162 | 25 | B | 7 | R17 | 147 |
| 10 | A | — | — | — | 26 | B | — | — | — |
| 11 | A | 157 | T15 | 163 | 27 | B | 6 | P16 | 148 |
| 12 | A | — | — | — | 28 | B | — | — | — |
| 13 | A | 156 | U14 | 164 | 29 | B | 5 | T17 | 149 |

Table 21. EPM7256E & EPM7256S I/O Pin-Outs (Part 2 of 5)

| MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP | MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP |
|----|-----|------------------------------|------------------------|----------------------|----|-----|------------------------------|------------------------|----------------------|
| 14 | A | — | U13 | 166 | 30 | B | — | N15 | 150 |
| 15 | A | — | — | — | 31 | B | — | — | — |
| 16 | A | 154 | T14 | 167 | 32 | B | 4 | T16 | 151 |
| 33 | C | 39 | B17 | 108 | 49 | D | 49 | A14 | 92 |
| 34 | C | — | — | — | 50 | D | — | — | — |
| 35 | C | 38 | C15 | 109 | 51 | D | 48 | B12 | 93 |
| 36 | C | — | — | — | 52 | D | — | — | — |
| 37 | C | 37 | C17 | 110 | 53 | D | 46 | B13 | 95 |
| 38 | C | — | C16 | 111 | 54 | D | — | A15 | 96 |
| 39 | C | — | — | — | 55 | D | — | — | — |
| 40 | C | 36 | D17 | 112 | 56 | D | 45 | B14 | 97 |
| 41 | C | 35 | D15 | 113 | 57 | D | 44 | A16 | 98 |
| 42 | C | — | — | — | 58 | D | — | — | — |
| 43 | C | 34 | E17 | 114 | 59 | D | 43 | C14 | 99 |
| 44 | C | — | — | — | 60 | D | — | — | — |
| 45 | C | 33 | D16 | 115 | 61 | D | 42 | B16 | 100 |
| 46 | C | — | E15 | 117 | 62 | D | — | B15 | 101 |
| 47 | C | — | — | — | 63 | D | — | — | — |
| 48 | C | 31 | F16 | 118 | 64 | D | 41 | A17 | 102 |
| 65 | E | 153 | U12 | 168 | 81 | F | 21 | J16 | 130 |
| 66 | E | — | — | — | 82 | F | — | — | — |
| 67 | E | 152 | R13 | 169 | 83 | F | 20 | J15 | 131 |
| 68 | E | — | — | — | 84 | F | — | — | — |
| 69 | E | 151 | U11 | 170 | 85 | F | 19 | K17 | 132 |
| 70 | E | — | T13 | 171 | 86 | F | — | J14 | 133 |
| 71 | E | — | — | — | 87 | F | — | — | — |
| 72 | E | 150 | T11 | 172 | 88 | F | 17 | K16 | 135 |
| 73 | E | 149 | T12 | 173 | 89 | F | 16 | K15 | 136 |
| 74 | E | — | — | — | 90 | F | — | — | — |
| 75 | E | 147 | R12 | 175 | 91 | F | 15 | L17 | 137 |
| 76 | E | — | — | — | 92 | F | — | — | — |
| 77 | E | 146 (3) | U10 (3) | 176 (3) | 93 | F | 14 | L16 | 138 |
| 78 | E | — | R10 | 177 | 94 | F | — | M17 | 139 |
| 79 | E | — | — | — | 95 | F | — | — | — |
| 80 | E | 145 | T10 | 178 | 96 | F | 13 | L15 | 140 |

Table 21. EPM7256E & EPM7256S I/O Pin-Outs (Part 3 of 5)

| MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP | MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP |
|-----|-----|------------------------------|------------------------|----------------------|-----|-----|------------------------------|------------------------|----------------------|
| 97 | G | 30 | E16 | 119 | 113 | H | 60 | C9 | 79 |
| 98 | G | — | — | — | 114 | H | — | — | — |
| 99 | G | 29 | F17 | 120 | 115 | H | 59 | D9 | 80 |
| 100 | G | — | — | — | 116 | H | — | — | — |
| 101 | G | 28 | F15 | 121 | 117 | H | 58 | C10 | 81 |
| 102 | G | — | G16 | 122 | 118 | H | — | A10 | 84 |
| 103 | G | — | — | — | 119 | H | — | — | — |
| 104 | G | 27 | G15 | 123 | 120 | H | 54 | A11 | 86 |
| 105 | G | 26 | G17 | 124 | 121 | H | 53 | B10 | 87 |
| 106 | G | — | — | — | 122 | H | — | — | — |
| 107 | G | 24 | H17 | 126 | 123 | H | 52 | A12 | 88 |
| 108 | G | — | — | — | 124 | H | — | — | — |
| 109 | G | 23 (3) | H15 (3) | 127 (3) | 125 | H | 51 | B11 | 89 |
| 110 | G | — | J17 | 128 | 126 | H | — | A13 | 90 |
| 111 | G | — | — | — | 127 | H | — | — | — |
| 112 | G | 22 | H16 | 129 | 128 | H | 50 | C12 | 91 |
| 129 | I | 128 | U6 | 197 | 145 | J | 100 | J2 | 27 |
| 130 | I | — | — | — | 146 | J | — | — | — |
| 131 | I | 129 | T5 | 196 | 147 | J | 101 | J3 | 26 |
| 132 | I | — | — | — | 148 | J | — | — | — |
| 133 | I | 130 | U7 | 195 | 149 | J | 102 | K1 | 25 |
| 134 | I | — | T6 | 194 | 150 | J | — | J4 | 24 |
| 135 | I | — | — | — | 151 | J | — | — | — |
| 136 | I | 131 | T7 | 193 | 152 | J | 104 | K2 | 22 |
| 137 | I | 132 | R6 | 192 | 153 | J | 105 | K3 | 21 |
| 138 | I | — | — | — | 154 | J | — | — | — |
| 139 | I | 134 | R7 | 190 | 155 | J | 106 | L1 | 20 |
| 140 | I | — | — | — | 156 | J | — | — | — |
| 141 | I | 135 (3) | U8 (3) | 189 (3) | 157 | J | 107 | L2 | 19 |
| 142 | I | — | R8 | 188 | 158 | J | — | M1 | 18 |
| 143 | I | — | — | — | 159 | J | — | — | — |
| 144 | I | 136 | T8 | 187 | 160 | J | 108 | L3 | 17 |

Table 21. EPM7256E & EPM7256S I/O Pin-Outs (Part 4 of 5)

| MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP | MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP |
|-----|-----|------------------------------|------------------------|----------------------|-----|-----|------------------------------|------------------------|----------------------|
| 161 | K | 91 | F3 | 38 | 177 | L | 61 | B9 | 78 |
| 162 | K | — | — | — | 178 | L | — | — | — |
| 163 | K | 92 | F1 | 37 | 179 | L | 62 | C8 | 77 |
| 164 | K | — | — | — | 180 | L | — | — | — |
| 165 | K | 93 | E2 | 36 | 181 | L | 63 | A9 | 76 |
| 166 | K | — | G2 | 35 | 182 | L | — | A8 | 73 |
| 167 | K | — | — | — | 183 | L | — | — | — |
| 168 | K | 94 | G3 | 34 | 184 | L | 67 | A7 | 71 |
| 169 | K | 95 | G1 | 33 | 185 | L | 68 | B8 | 70 |
| 170 | K | — | — | — | 186 | L | — | — | — |
| 171 | K | 97 | H1 | 31 | 187 | L | 69 | A6 | 69 |
| 172 | K | — | — | — | 188 | L | — | — | — |
| 173 | K | 98 (3) | H3 (3) | 30 (3) | 189 | L | 70 | B7 | 68 |
| 174 | K | — | J1 | 29 | 190 | L | — | A5 | 67 |
| 175 | K | — | — | — | 191 | L | — | — | — |
| 176 | K | 99 | H2 | 28 | 192 | L | 71 | C6 | 66 |
| 193 | M | 119 | U1 | 4 | 209 | N | 109 | N1 | 16 |
| 194 | M | — | — | — | 210 | N | — | — | — |
| 195 | M | 120 | R2 | 3 | 211 | N | 110 | M2 | 15 |
| 196 | M | — | — | — | 212 | N | — | — | — |
| 197 | M | 121 | R3 | 206 | 213 | N | 112 | M3 | 13 |
| 198 | M | — | U2 | 205 | 214 | N | — | P1 | 12 |
| 199 | M | — | — | — | 215 | N | — | — | — |
| 200 | M | 122 | P4 | 204 | 216 | N | 113 | N2 | 11 |
| 201 | M | 123 | U3 | 203 | 217 | N | 114 | R1 | 10 |
| 202 | M | — | — | — | 218 | N | — | — | — |
| 203 | M | 124 | T3 | 202 | 219 | N | 115 | P2 | 9 |
| 204 | M | — | — | — | 220 | N | — | — | — |
| 205 | M | 125 | U4 | 201 | 221 | N | 116 | T1 | 8 |
| 206 | M | — | U5 | 199 | 222 | N | — | N3 | 7 |
| 207 | M | — | — | — | 223 | N | — | — | — |
| 208 | M | 127 | T4 | 198 | 224 | N | 117 | T2 | 6 |

Table 21. EPM7256E & EPM7256S I/O Pin-Outs (Part 5 of 5)

| MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP | MC | LAB | 160-Pin PQFP, (1), (2) | 192-Pin PGA, (2) | 208-Pin RQFP/PQFP |
|-----|-----|------------------------------|------------------------|----------------------|-----|-----|------------------------------|------------------------|----------------------|
| 225 | O | 82 | B1 | 49 | 241 | P | 72 | A4 | 65 |
| 226 | O | — | — | — | 242 | P | — | — | — |
| 227 | O | 83 | C3 | 48 | 243 | P | 73 | B6 | 64 |
| 228 | O | — | — | — | 244 | P | — | — | — |
| 229 | O | 84 | C1 | 47 | 245 | P | 75 | B5 | 62 |
| 230 | O | — | D3 | 46 | 246 | P | — | A3 | 61 |
| 231 | O | — | — | — | 247 | P | — | — | — |
| 232 | O | 85 | D1 | 45 | 248 | P | 76 | B4 | 60 |
| 233 | O | 86 | C2 | 44 | 249 | P | 77 | A2 | 59 |
| 234 | O | — | — | — | 250 | P | — | — | — |
| 235 | O | 87 | E1 | 43 | 251 | P | 78 | C4 | 58 |
| 236 | O | — | — | — | 252 | P | — | — | — |
| 237 | O | 88 | E3 | 42 | 253 | P | 79 | B2 | 57 |
| 238 | O | — | D2 | 40 | 254 | P | — | B3 | 56 |
| 239 | O | — | — | — | 255 | P | — | — | — |
| 240 | O | 90 | F2 | 39 | 256 | P | 80 | A1 | 55 |

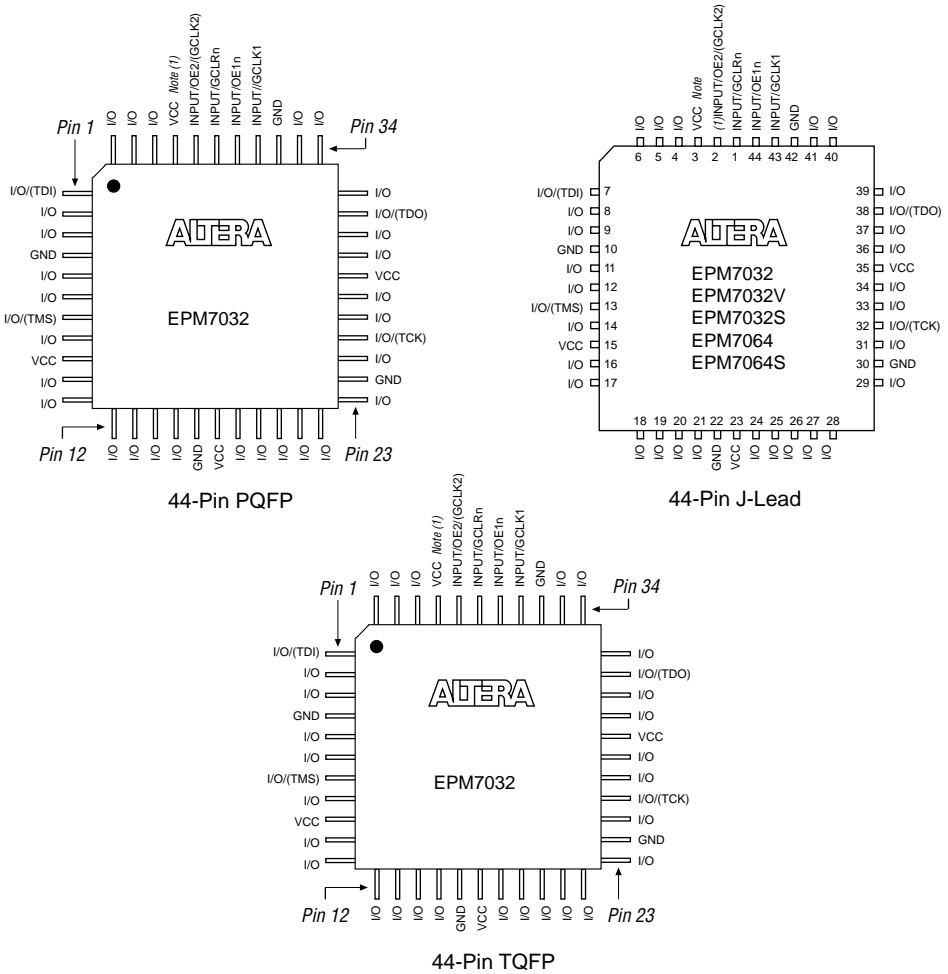
Notes to tables:

- (1) A complete thermal analysis should be performed before committing a design to this device package. See the *Operating Requirements for Altera Devices Data Sheet* in the **1998 Data Book** for more information.
- (2) This package is not available in EPM7256S devices.
- (3) This JTAG pin applies to only MAX 7000S devices. For MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Figures 18 through 24 show the package pin-out diagrams for MAX 7000 devices.

Figure 18. 44-Pin Package Pin-Out Diagram

Package outlines not drawn to scale. Pin functions shown in parentheses are for MAX 7000S devices only.



Note:

(1) This pin is a power-down pin (PDn) for EPM7032V devices.

Figure 19. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale. Pin functions shown in parentheses are for MAX 7000S devices only.

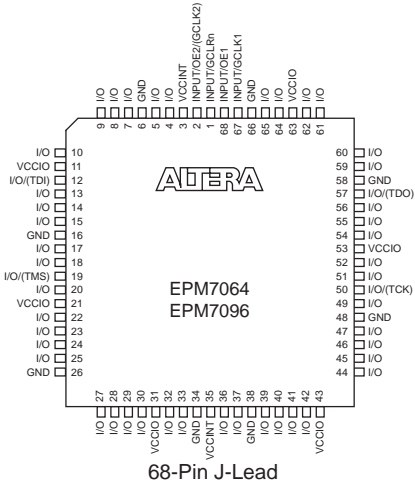
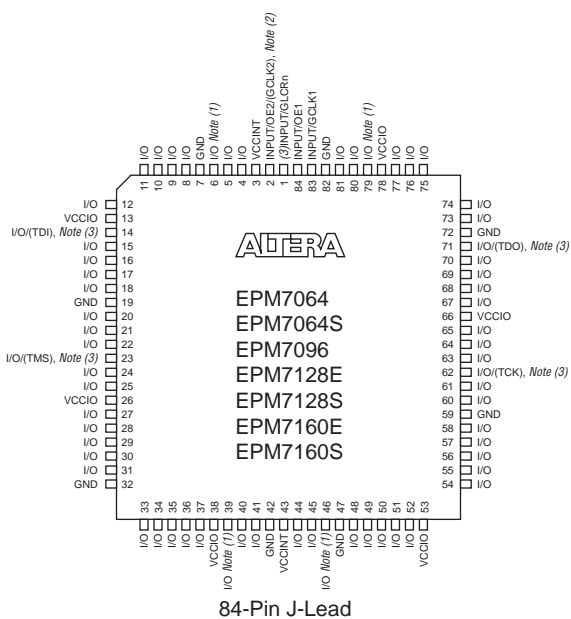


Figure 20. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale. Pin functions in parentheses are for MAX 7000S devices only.



Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) These pins are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are only available in MAX 7000S devices.

Figure 21. 100-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

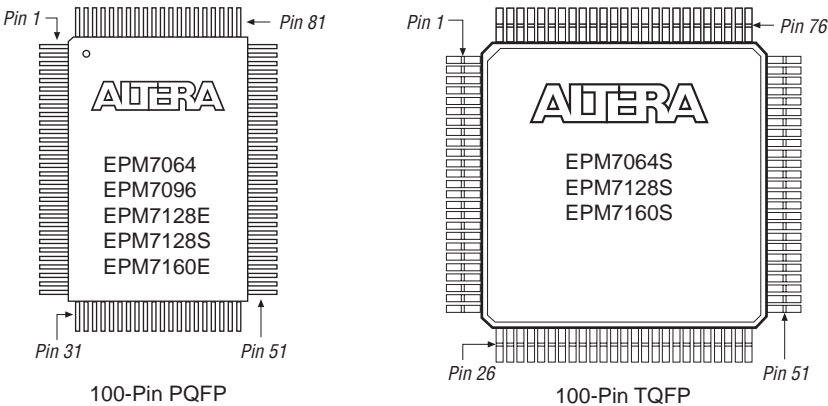


Figure 22. 160-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

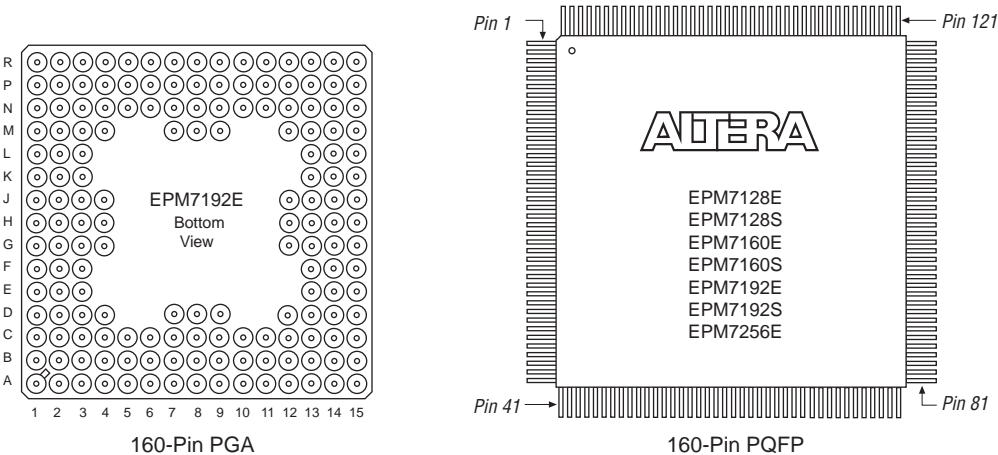


Figure 23. 192-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

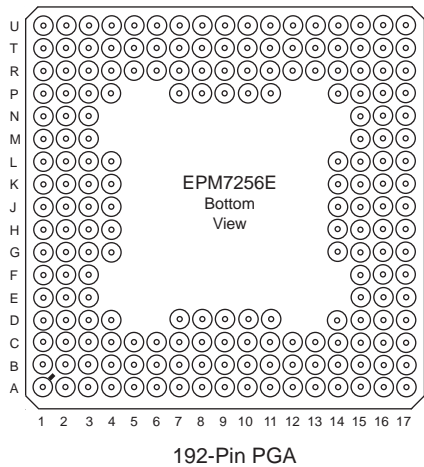
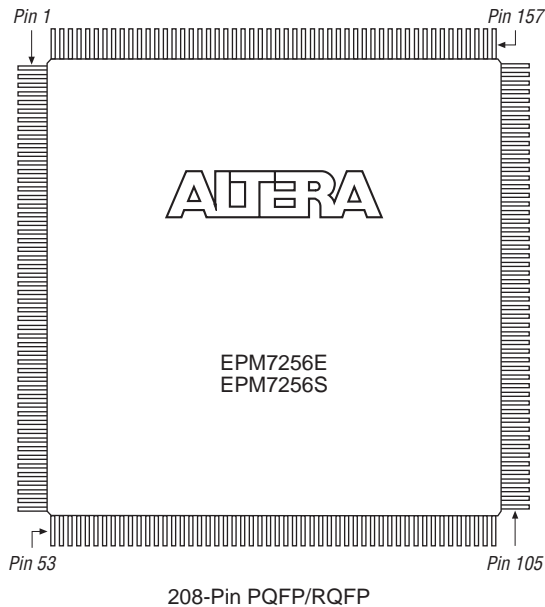


Figure 24. 208-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 5.03 supersedes information published in previous versions.

Version 5.03 Changes

The *MAX 7000 Programmable Logic Device Family Data Sheet* version 5.03 contains the following change:

- Throughout the document, clarified which devices support JTAG BST.

Version 5.02 Changes

The *MAX 7000 Programmable Logic Device Family Data Sheet* version 5.02 contained the following changes:

- Added description of “F” suffix devices to the “**In-System Programmability (ISP)**” section on page 16.

Version 5.01 Changes

The *MAX 7000 Programmable Logic Device Family Data Sheet* version 5.01 contained the following changes:

- Added detailed information on I/O operation to the “**In-System Programmability (ISP)**” section on page 16.
- Added missing data on V_{OH} and V_{OL} operation to the MAX 7000 5.0-V Device DC Operating Conditions table.
- Added note to **Table 6** regarding preliminary status to applicable MAX 7000 devices.
- Corrected Note (3) to Note (4) for the P_{Dn} pin in **Table 7**.
- Added missing GND pins to **Table 14**.
- Made minor textual, illustration, and style changes to the data sheet.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 894-7104
Literature Services:
(888) 3-ALTERA
lit_req@altera.com

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